Troubleshooting USB 2.0 Problems with Your Oscilloscope

APPLICATION NOTE

Tektronix®

Introduction

USB-based systems are all around us, both in embedded systems where USB is used as an interconnect technology between components inside a product, and as a popular external interconnect bus between computer and peripheral devices. An extra benefit of the USB interface is that it supports delivery of power from the host to peripheral devices.

The Universal Serial Bus (USB) has become a dominant interface on today's personal computers, replacing many of the external serial and parallel buses previously used. Since its introduction in 1995, USB has grown beyond its original personal computer usage and has become a ubiquitous interface used in many types of electronic devices.

USB has expanded beyond just system-to-system communication. For example, the Inter-Chip USB (IC_USB) and the High-Speed Inter-Chip (HSIC) USB are used for chip-to-chip communications.

USB 2.0 is a mature standard and many of the building blocks are robust. However, these buses can be impacted by noise, board layout, termination and other factors. In case of bus communication failures, an oscilloscope is the go-to tool for providing timing and amplitude information initially, and when equipped with decoding capability, also protocol-level diagnostic information.

Even when the USB bus is operating correctly, other systems can suffer problems under specific conditions. In these cases triggering on specific USB bus values can provide a critical time reference to help troubleshoot system-level bugs.

THIS APPLICATION NOTE

- Gives a brief orientation on the physical layer and packet structures of USB 2.0, with the goal of providing just enough detail to help with troubleshooting
- Explains how to set up decoding on an oscilloscope equipped with USB 2.0 decoding
- Explains how to interpret serial bus data on an oscilloscope equipped with USB 2.0 decoding
- Explains what triggering and searching options are available on an oscilloscope equipped with USB2.0 serial decode capability

With optional serial triggering and analysis capability, Tektronix oscilloscopes become powerful tools for embedded system designers working with USB 2.0 buses. In this application note the 5 Series MSO is used to demonstrate USB serial bus decoding and triggering.

Support for serial bus standards vary depending on the oscilloscope model. For a table of buses supported by different Tektronix oscilloscopes, please see Appendix A or visit www.tektronix.com.

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USB 2.0

BACKGROUND

The USB 2.0 specification released in 2000 covers most of the USB devices that are being used today. USB 2.0 replaced the USB 1.1 specification, adding a high-speed interface to the low-speed and full-speed interfaces defined in the USB 1.1 specification. Supplements to the USB 2.0 specification cover IC_USB, HSIC and other enhancements.

In 2008, the USB 3.0 specification was released. USB 3.0 is called SuperSpeed USB and is ten times faster than high-speed USB 2.0. SuperSpeed USB preserves backward compatibility with USB 2.0 devices. USB 3.0 is an additional specification that is used in conjunction with the USB 2.0 specification and does not replace it. SuperSpeed USB devices must implement USB 2.0 device framework commands and descriptors.

The USB Implementers Forum (USB-IF) manages and promotes USB standards and USB technology. USB specifications are available at the USB-IF web site at www.usb.org.

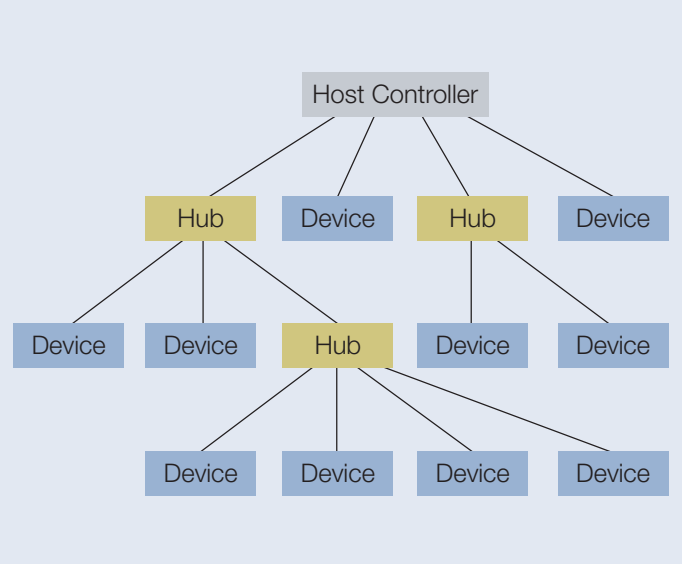
HOW IT WORKS

USB SPEED	BIT RATE	BIT PERIOD
Low-Speed USB 2.0	1.5 Mb/s	667 ns
Full-Speed USB 2.0	12 Mb/s	83.3 ns
High-Speed USB 2.0	480 Mb/s	2.08 ns
SuperSpeed USB 3.0	5 Gb/s	200 ps

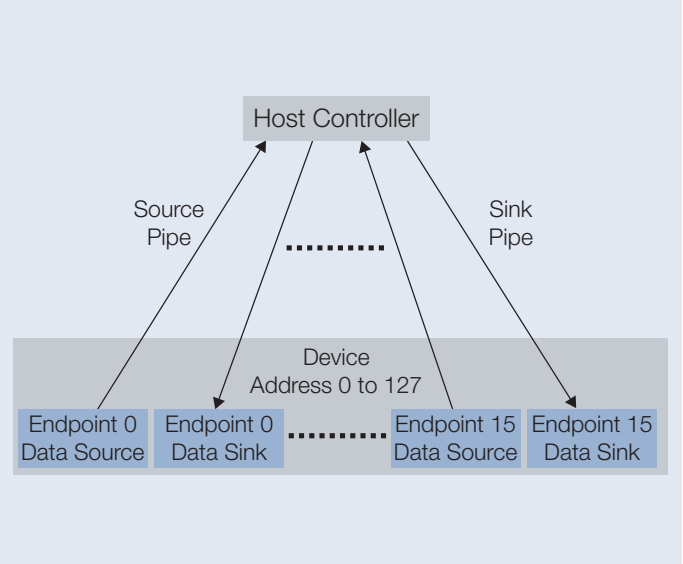
There are four USB speeds. A high-speed device starts out at full-speed and then transitions to high-speed. The speed of a USB 2.0 bus is limited by the slowest device connected to the host controller.

With SuperSpeed USB, two host controllers are used: one for SuperSpeed USB devices and one for USB 2.0 devices. Like a USB 2.0 system, the speed of the bus with USB 3.0 devices is limited by the slowest device.

USB serial triggering and analysis support is available on select Tektronix oscilloscopes (see Appendix A). For low- speed and full-speed USB, trigger, decode and search support is provided by all of the oscilloscope models. For high-speed USB signals, a ≥1 GHz oscilloscope model is required.



A USB network includes one host controller and from 1 to 127 devices. USB is a tiered-star topology with optional hubs to expand the bus. The host is the only master and it controls all bus traffic. The host initiates all device communications and devices do not have the capability to interrupt the host.



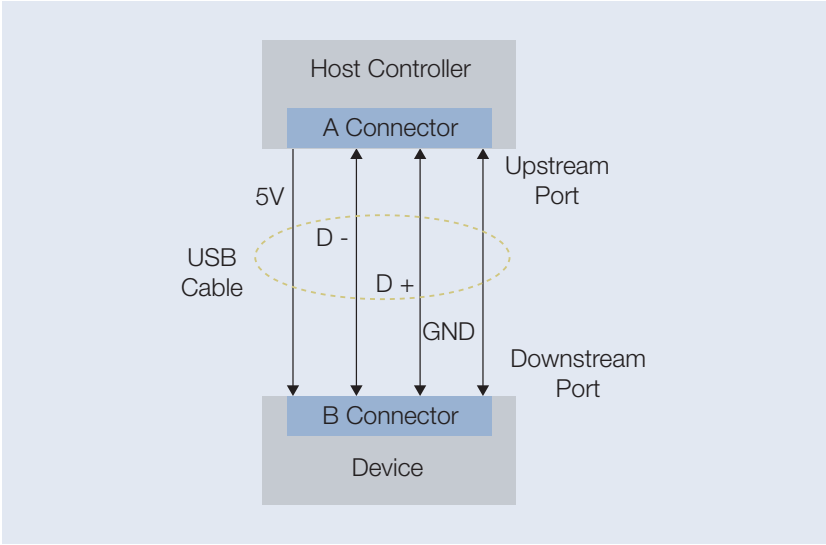
Each device can have up to 16 data endpoints. Device endpoints are data sources and sinks in the device. Endpoint 0 is mandatory and is used by the host to communicate to the device. A pipe is the logical connection between the application software in the host and device endpoint.

The connections in a USB network are configured dynamically during an enumeration process which occurs at power-on or when a device is hot-plugged. The sequence is as follows:

1. The host detects the presence of the device on the USB bus.
2. The host polls the device with the SETUP token using address 0 and endpoint 0.
3. The host assigns a unique address to the device in the range of 1 to 127.
4. The host identifies the device speed and data transfer type.
5. The device's class is determined. The device class defines a device's functionality such as printer, mass storage, video, audio, human interface, etc.

ELECTRICAL INTERFACE

The host incorporates an upstream “A” connector and devices have a downstream “B” connector. Each connector has three versions: standard, mini, and micro. The USB 2.0 cable has four wires: two wires are used to provide power from the host: 5 V power (red wire) and ground (black wire). The connectors are designed so that the power and ground pins are connected before the data pins. The host provides current from 100 mA to 500 mA with intelligent power management. For example, power to a device can be monitored by the host or hub and switched off if an over-current condition occurs.



A twisted differential pair Data+ (D+ green wire) and Data- (D- white wire) wires are used for bidirectional communications using half-duplex differential signaling controlled by the host. On an oscilloscope the individual signals can be captured using passive or active analog probes, as well as digital logic probes.

SIGNALING

USB SPEED	LOW STATE	HIGH STATE
Low-Speed	<0.3V	>2.8V
Full-Speed	<0.3V	>2.8V
High-Speed	0 V±10%	400 mV±10%
SuperSpeed USB 3.0	5 Gb/s	200 ps

Voltage levels are nominally equivalent for low-speed and full-speed devices, but they are significantly lower for high-speed devices. When no device is connected, the host pulls down both D+ and D-. This is called single-ended zero (SE0) state. When a device is connected to the bus, pull-up resistors indicate the initial speed of the device.

DATA STATES	DIFFERENTIAL VOLTAGE
J State	Low-speed device: drives D- high for negative differential voltage
	High/Full-speed device: drives D+ high for positive differential voltage
K State	Low-speed device: drives D+ high for a positive differential voltage
	High/Full-speed device: drives D- high for a positive differential voltage

Data transmission uses non return to zero inverted (NRZI) encoding and the two data states are referred to as J and K. The differential voltages representing the J state and K state are of opposite polarity for low and full-speed devices. To ensure a minimum number of transitions, the standard requires bit stuffing. The least significant bit is transmitted first and the most significant bit is transmitted last.

PACKETS

Packets are the fundamental elements of USB communications. Packets start with a synchronization field followed by the packet identifier. Depending upon the type of packet, the packet identifier may be followed by additional fields or no field, depending upon the type of packet. The end-of-packet field terminates the packet.

K	J	K	J	K	J	K	K

Starting from the J idle state, a packet starts with an 8-bit synchronization (SYNC) field for low-speed and full-speed USB. SYNC is 3 KJ pairs followed by two Ks.

The SYNC field for high-speed USB is 15 KJ pairs followed by two Ks and hubs are allowed to reduce the repeating SYNC field to 5 KJ pairs followed by two Ks.

The packet identifier (PID) is the second packet byte composed of a 4-bit PID and its 4-bit PID complement for error checking. The PID 4-bit value identifies 17 types of packets. Packet type groups are token, data, handshake and special.

A PID encoding error occurs when the first PID 4-bits do not match the complement of the last PID 4-bits. Bits are sent out onto the bus least-significant bit first and most-significant bit last.

The end-of-packet (EOP) is three bits long. EOP starts with two bits of SE0 and ends with one bit of J state.

USB PACKET TYPE	PACKET	BINARY VALUE
Token	OUT	0001
	IN	1001
	SOF	0101
	SETUP	1101
Data	DATA0	0011
	DATA1	1011
	DATA2	0111
	MDATA	1111
Handshake	ACK	0010
	NAK	1010
	STALL	1110
	NYET	0110
Special	PRE	1100
	ERR	1100
	SPLIT	1000
	PING	0100
	Reserved	0000

Handshake Packets

Handshake packets such as data packet accepted (ACK) and data packet not accepted (NAK) are composed of the SYNC byte, PID byte, and EOP.

Token Packets

Host-sent token packets are composed of the SYNC, PID followed by two bytes composed of an 11-bit address and 5-bit cyclic redundancy check (CRC).

The OUT, IN, and SETUP tokens' 11-bit address is subdivided into a 7-bit device address and a 4-bit endpoint identifier.

Address zero is special and is for a device that has not been assigned an address at the beginning of the enumeration process. Later in the enumeration process the host assigns a nonzero address to the device.

All devices have an endpoint zero. Endpoint zero is used for device control and status. Other device endpoints are for data sources and/or sinks.

The host sends an OUT token to a device followed by a data packet. The host sends an IN token to a device and expects to receive a data packet or handshake packet such as NAK from the device.

Data Packets

Data packets contain a PID byte, data bytes and 16-bit CRC.

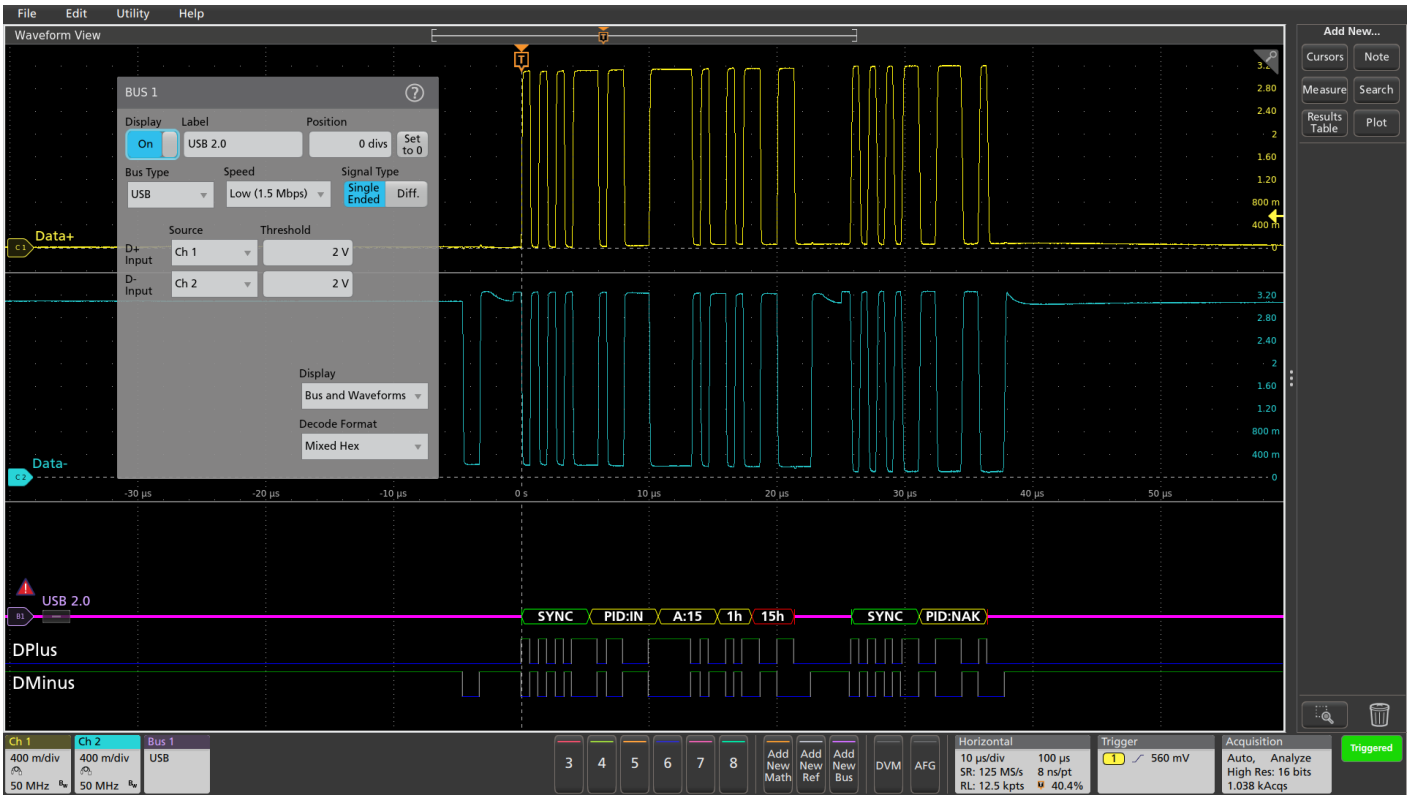
DATA0 and DATA1 packets have a 1-bit sequence number that is used in stop and wait automatic repeat-request handshake. DATA0 and DATA1 packets alternate in error free transmission. Data packets are resent with the same sequence number when a transmission error occurs.

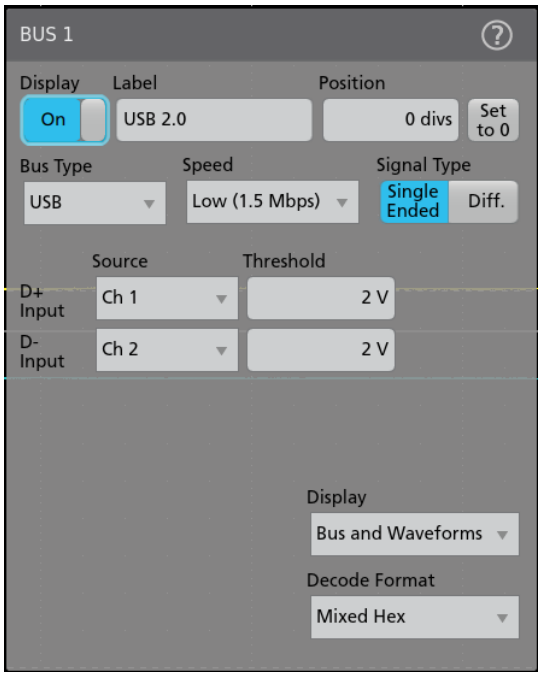
An error-free data transaction is when the host sends a DATA0 packet to the device, the device sends a handshake ACK packet and then the host sends a DATA1 packet.

If the host does not receive a handshake ACK packet or received a NAK from the device, it resends the DATA0 packet. If the device sent an ACK packet and receives the data packet with the same sequence number, the device acknowledges the data packet but ignores the data as a duplicate.

Start of Frame

A Start of Frame (SOF) packet is used to synchronize isochronous and polled data flows. The 11-bit frame number is incremented by one in each consecutive SOF.





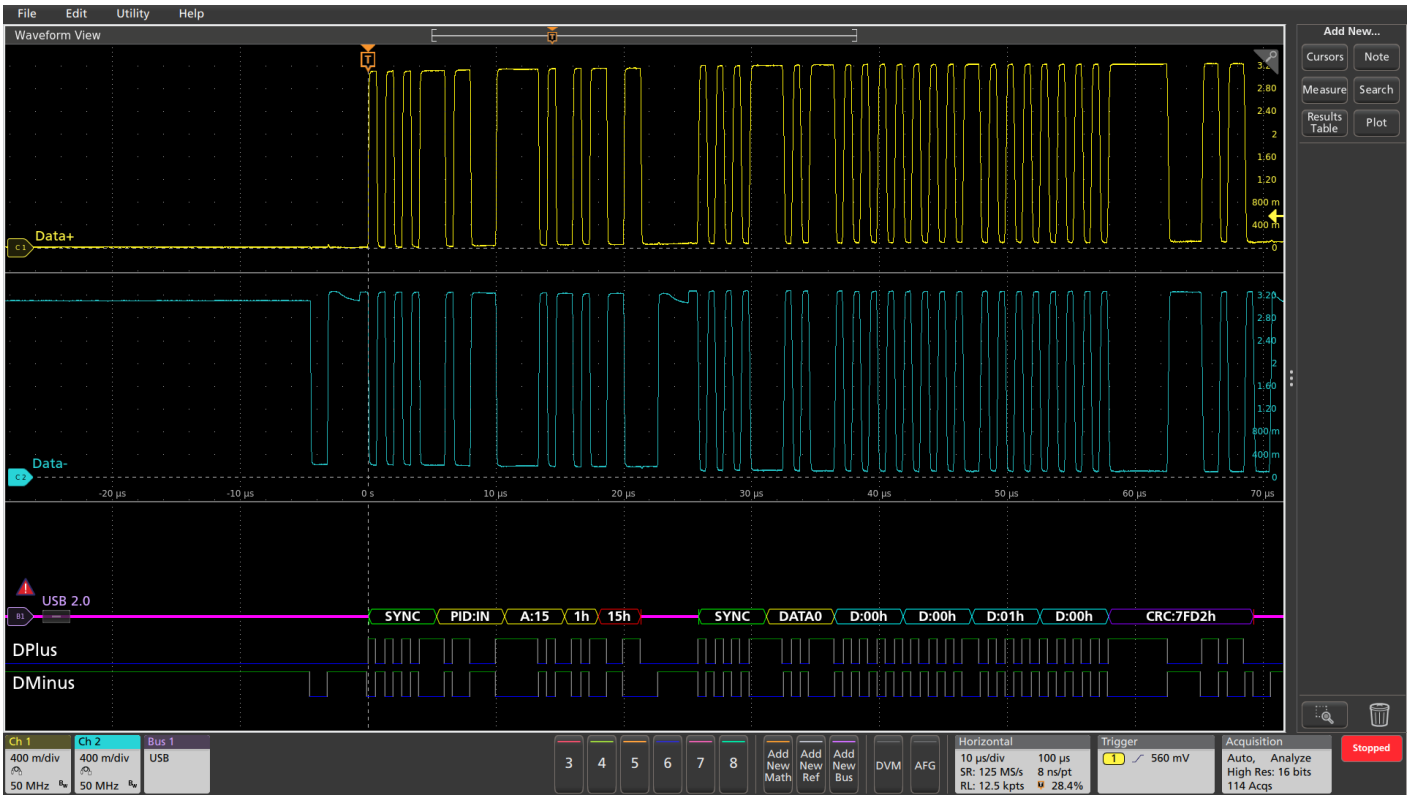
Setting up USB 2.0 Decoding

By tapping the Add New Bus button or pushing the front panel Bus button, we can define a USB bus by simply entering the basic parameters of the bus including the signal speed, the input channel(s), the signal type, and voltage threshold(s).

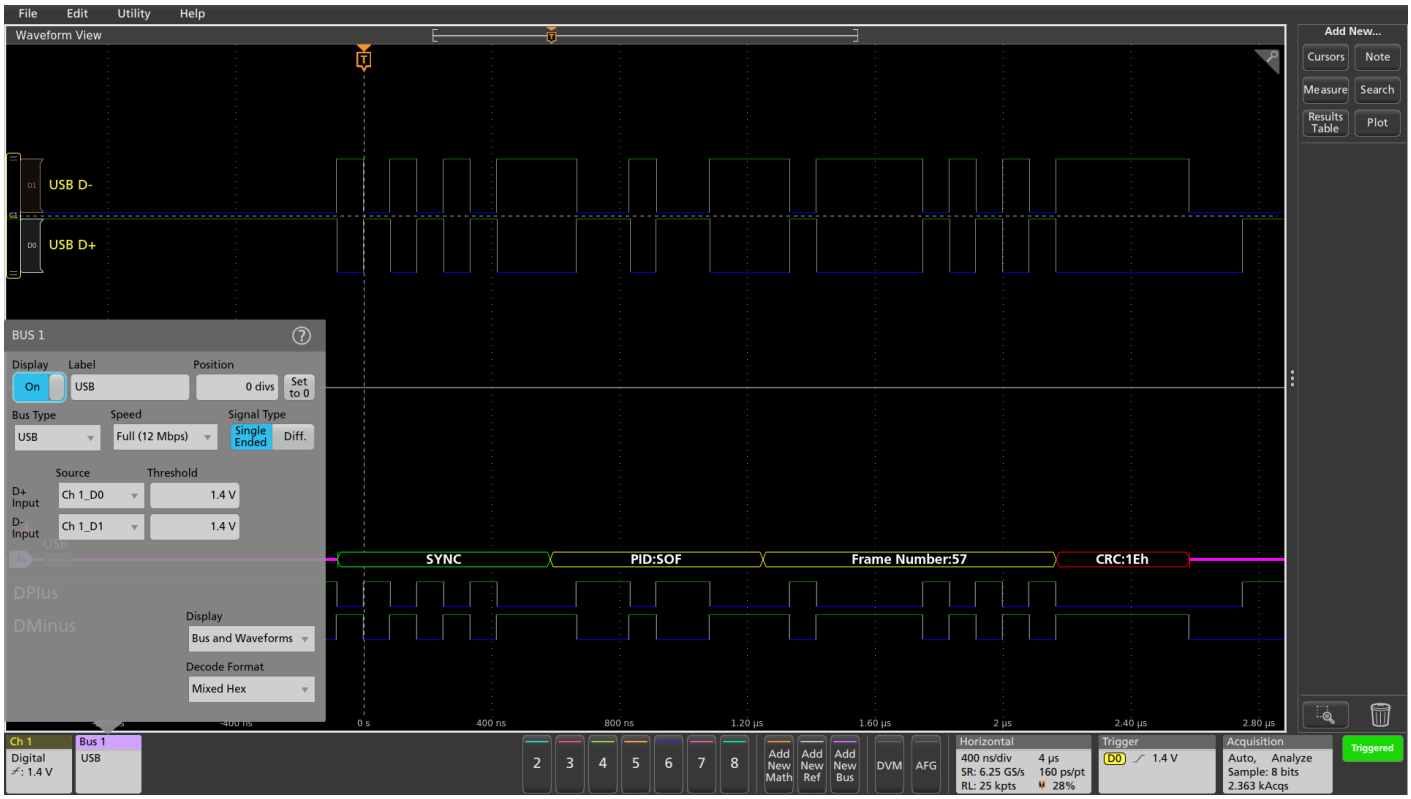
USB 2.0 signals are transmitted as a differential pair. The individual signals can be captured using passive or active analog probes, as well as digital logic probes. As shown in the configuration menu to the left, two single-ended analog inputs are set up to capture the low-speed USB 2.0 traffic between a PC and a mouse.

INTERPRETING THE USB 2.0 BUS

The oscilloscope shows communication between a host and low-speed USB mouse, including the setup. The USB host sends an IN token, requesting data, and the mouse responds with a NAK, since the mouse has not moved.

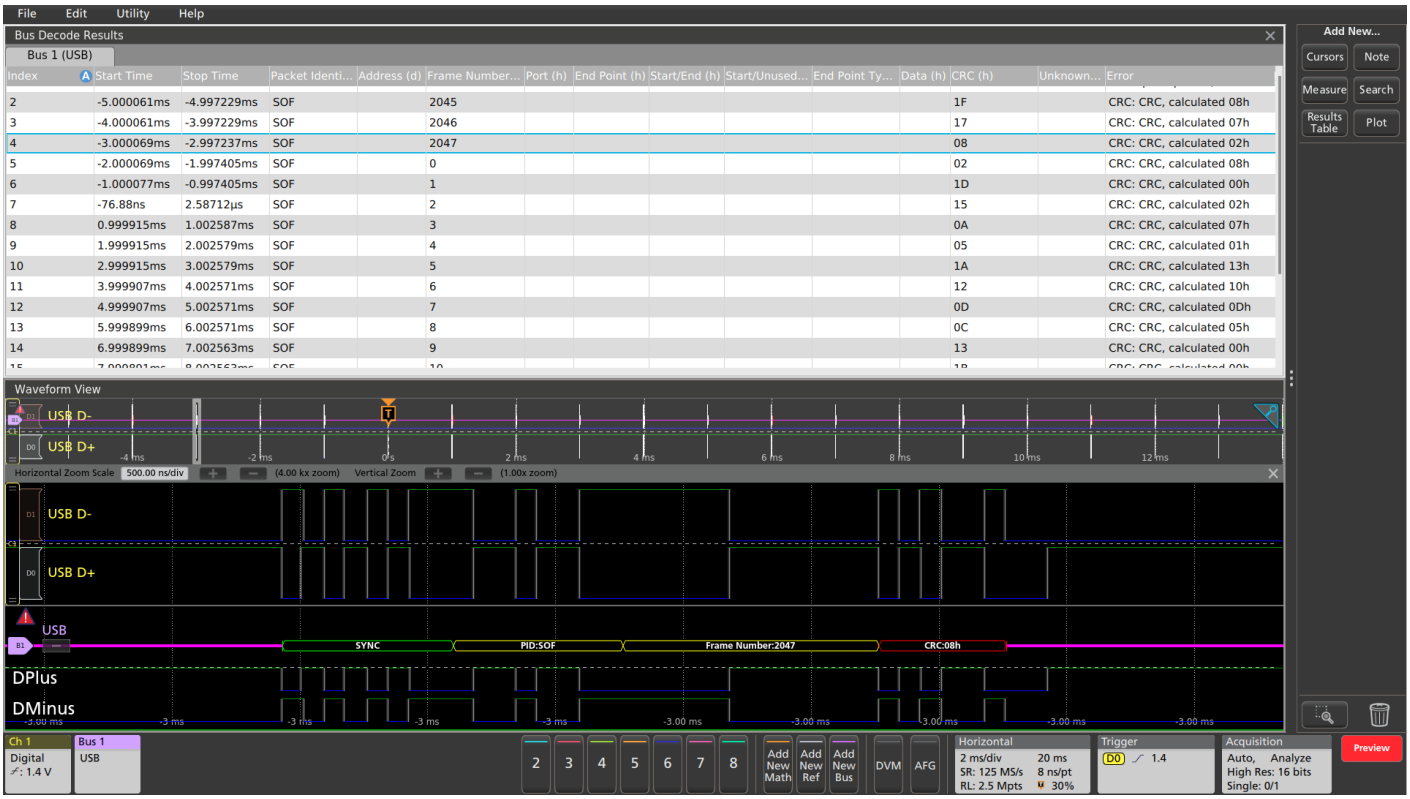


When the mouse is moved, it responds to the host request with a series of data bytes indicating the change of position.



This case shows full-speed USB 2.0 traffic between a PC and a USB drive. A logic probe connected to a FlexChannel® input is used to capture the signals. Although the oscilloscope can acquire and decode lower-speed USB bus signals using single-ended probing, the signal fidelity and noise immunity is improved by using differential probing, and is a necessity for high-speed USB signals.

USB 2.0 BUS ELEMENT	INDICATED BY
Start of frame	
Sync field	SYNC
Packet Identifier indicates the type of packet	PID:IN
Addresses	Addr:15
Data values can be displayed in either hex or binary	D:00h
CRC values are shown in purple boxes. CRC errors are shown in red boxes	CRC:15h
End Of Frame	



For firmware engineers, the Results Table format may be more useful. This time-stamped display of bus activity can be easily compared to the software listings, and provides easy calculation of the execution speed.

The Results Table also provides linkage back to the waveform displays. You can tap a line in the tabular display and the oscilloscope automatically zooms in on the corresponding bus signals and resulting decoded bus waveform, shown in the lower section of the screen.

TRIGGERING ON THE USB 2.0 BUS

The next step in debugging or validating a design is setting up the oscilloscope to isolate, capture, and display a specific bus event of interest.

In this example, a differential probe is used to probe a USB extension cable between a PC and a high-speed USB memory device. The oscilloscope is triggering on a data packet beginning with the 16-bit value of 12 01 hex.

The oscilloscope can trigger on the following USB bus elements:

TRIGGER ON	DESCRIPTION
Sync	Synchronization field
Handshake Packet	Specify any of these types: Any, ACK, NAK, STALL, NYET
Special Packet	Specify any of these types: Any, ERR, SPLIT, PING, RESERVED
Error	Specify and of these types: PID Check Bits, Token CRC5, Data CRC16, or Bit stuffing
Token (Address) Pack et	Specify and of these types: Any, SOF, OUT, IN, SETUP
Data Packet	Specify and of these types: Any, DATA0, DATA1, DATA2, MDATA, up to a 16-byte data pattern
Reset	
Suspend	
Resume	
End of Packet (EOP)	

SEARCHING ON THE USB 2.0 BUS

On a Tektronix oscilloscope you can configure Wave Inspector to automatically search and mark the same events as specified for triggering. For example, Wave Inspector can search through the entire acquisition looking for every instance of a SETUP token packet with address 00 hex. In this case, Wave Inspector found 2 instances of the specified bus event. Each marked event is easily viewed by using the Wave Inspector front-panel Navigate buttons to jump between events.

Appendix A

TEKTRONIX OFFERS A RANGE OF MODELS TO MEET YOUR NEEDS AND YOUR BUDGET:

	MSO/DPO70000 SERIES	DPO7000C SERIES	5 SERIES MSO	MSO/DPO5000 SERIES	MDO4000C SERIES	MDO3000 SERIES	MSO/DPO2000 SERIES
Bandwidth	33 GHz, 25 GHz, 23 GHz, 20 GHz, 16 GHz, 12.5 GHz, 8 GHz, 6 GHz, 4 GHz	3.5 GHz, 2.5 GHz, 1 GHz, 500 MHz	2 GHz, 1 GHz, 500 MHz, 350 MHz	2 GHz, 1 GHz, 500 MHz, 350 MHz	1 GHz, 500 MHz, 350 MHz, 200 MHz	1 GHz, 500 MHz, 350 MHz, 200 MHz, 100 MHz	200 MHz, 100 MHz, 70 MHz
Analog Channels	4	4	4, 6, 8	4	4	2 or 4	2 or 4
Digital Channels	16 (MSO)	--	8 to 64 (opt.)	16 (MSO)	16 (opt.)	16 (opt.)	16 (MSO)
Spectrum Analyzer Channels	--	--	--	--	1 (opt.)	1	--
Record Length (All Channels)	Up to 62.5 M (std.) Up to 250 M (opt.)	25 M (std.) Up to 125 M (opt.)	62.5 M (std.) 125 M (opt.)	25 M (std.) Up to 125 M (opt.)	20 M	10 M	1 M
Sample Rate (Analog)	Up to 100 GS/s	Up to 40 GS/s	Up to 6.25 GS/s	Up to 10 GS/s	Up to 5 GS/s	Up to 5 GS/s	1 GS/s
Color Display	12.1 in. XGA	12.1 in. XGA	15.6 in. HD	10.4 in. XGA	10.4 in. XGA	9 in. WVGA	7 in. WQVGA
Serial Bus Triggering and Analysis	I^2C SPI RS-232/422/485/ UART CAN LIN FlexRay USB 2.0 10/100BASE-T Ethernet MIL-STD-1553 8b/10b decoding D-PHY MIPI decoding PCI Express decoding	I^2C SPI RS-232/422/485/ UART CAN LIN FlexRay USB 2.0 10/100BASE-T Ethernet MIL-STD-1553 8b/10b decoding D-PHY MIPI decoding PCI Express decoding	I^2C SPI RS-232/422/485/ UART CAN LIN FlexRay USB 2.0 10/100BASE-T Ethernet I^2S/LJ/RJ/TDM	I^2C SPI RS-232/422/485/ UART CAN LIN FlexRay USB 2.0 10/100BASE-T Ethernet MIL-STD-1553 8b/10b decoding D-PHY MIPI decoding PCI Express decoding	I^2C SPI RS-232/422/485/ UART CAN CAN FD LIN FlexRay USB 2.0 I^2S/LJ/RJ/TDM MIL-STD-1553	I^2C SPI RS-232/422/485/ UART CAN CAN FD LIN FlexRay USB 2.0 I2S/LJ/RJ/TDM MIL-STD-1553	I^2C SPI RS-232/422/485/ UART CAN LIN
Number of Simultaneously Displayed Serial Buses	16	16	Essentially unlimited	16	3	2	2

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