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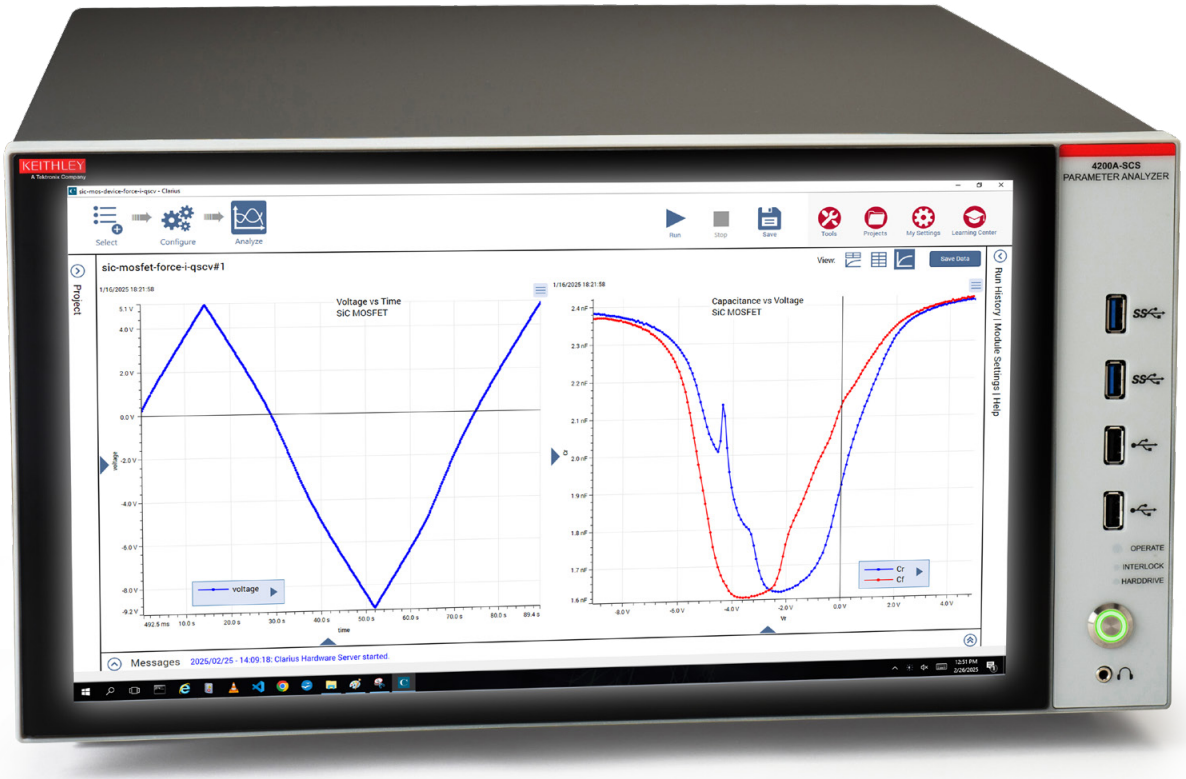
Forced Current Quasistatic C-V Method for SiC Devices

APPLICATION NOTE



Introduction

Capacitance voltage (C-V) measurements are used for analyzing semiconductor materials and in semiconductor device fabrication. C-V is particularly useful for characterizing Metal-Oxide-Semiconductors (MOS). Some of the many MOS device properties extracted from C-V data include mobile charges in the oxide, oxide capacitance, interface traps, doping profile, flat band voltage, doping concentration, minority carrier lifetime and input/output capacitances.

For most semiconductor C-V measurements, high frequency (typically 100 kHz to 1 MHz) is used. However, for some C-V measurements, a low frequency, or quasistatic, technique is required. This is the case for interface trap density (DIT) measurements on a MOScap, where quasistatic C-V is able to detect interface traps. For Si MOSFETs, a charge pumping technique can be used for determining DIT. At high frequency, interface traps cannot change state rapidly enough to contribute to the device capacitance. As a result, both the high and low frequency measurements are required to determine the number of trapped charges.

Available quasistatic C-V solutions usually involve forcing a voltage and measuring current using a source measure unit (SMU). These techniques can be effective on traditional silicon MOS devices. However, with SiC MOS devices, the higher capacitance makes these ammeter techniques difficult to use because the higher capacitance can cause unstable results.

To avoid problems caused by measuring current and stepping voltages in quasistatic methods, the Keithley 4200A-SCS Parameter Analyzer uses the Forced Current Quasistatic C-V (Force-I QSCV) technique. This method forces current, measures voltage and time, and derives the capacitance. Some of the advantages to using the Force-I QSCV technique on a SiC power MOS device include:

- Requires only one SMU with a preamp (other methods use two).
- Forcing current is faster than force voltage methods.
- Forcing constant DC current to the DUT allows for a steady state condition unlike stepping voltages.
- Measures voltage: avoids instability problems when using an instrument in low output impedance mode to derive the capacitance.
- Calculates capacitance from the following equation:

$$I = C * \frac{dV}{dt}$$

- Performs open correction.
- Corrects for leakages.
- Provides similar results to C-V measurements taken with the Keithley 595 Quasistatic C-V Meter.
- Investigating if DIT can be extracted using forward and reverse curves.
- This technique works on larger capacitances > 20 pF.

Beginning with the Clarius V1.14 Software release, tests that perform the Force-I QSCV technique are included with the Clarius Software that comes with the Keithley 4200A-SCS. These tests are some of many included in the extensive test library provided in the 4200A-SCS Clarius+ Software Suite. A single SMU with a preamp is required to run the Force-I QSCV tests in Clarius.

This application note describes the Force-I QSCV technique, explains how to use the tests in the Clarius Software, compares this technique to other methods and derives calculations for internal charges on a SiC MOSFET from the forward and reverse C-V sweeps.

Force-I QSCV Technique Using Three Steps

The Force-I QSCV technique uses a single SMU with a preamp to derive the quasistatic C-V characteristics of a SiC MOSFET or MOScap. An SMU is an instrument that sources and measures current and voltage. As shown in **Figure 1**, the force HI terminal of the SMU is connected to the gate of the power MOSFET, and the force LO terminal of the SMU is connected to the drain and source terminals shorted together.

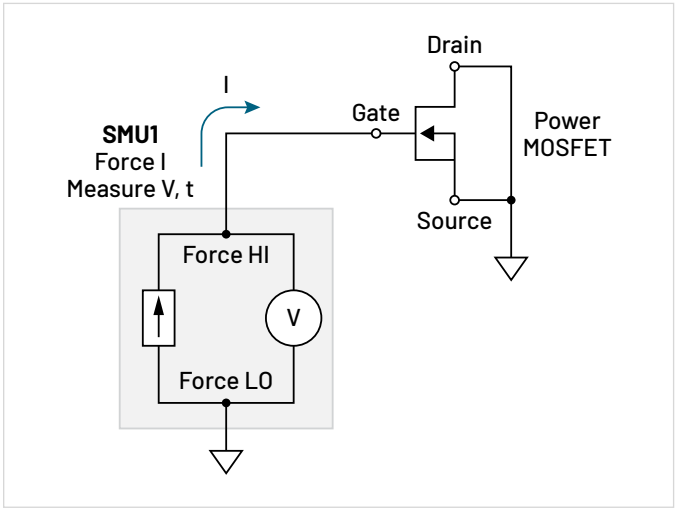


Figure 1. A power MOSFET is connected between the force HI and force LO terminals of the SMU.

The forced current quasistatic C-V method derives forward and reverse C-V curves using a three-step method by forcing positive and negative current while measuring voltage as a function of time. The constant current provides accurate control of the total charge ($Q=\sum I*dt$) supplied to the device. Using constant current allows for a steady state condition for the instrument unlike voltage stepping that can cause dynamic changes in the measurement equipment. The voltage and current timing diagrams of the three steps are illustrated in **Figure 2** and are further explained in the paragraphs that follow.

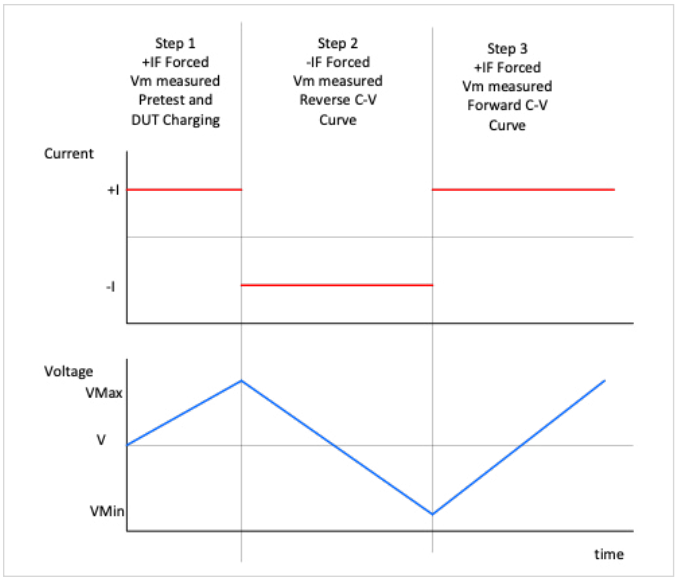


Figure 2. Current and voltage timing diagrams for Force-I QSCV test.

Step 1. The SMU forces a constant current (+I) and measures the voltage (V) and time until the voltage reaches a user defined maximum level, VMax. This step charges the device. The readings taken during this step are not used for the capacitance measurements.

Step 2. After VMax is reached, the polarity of the current source changes to -I and the voltage is measured until the predefined VMin is reached. During this step, the reverse C-V (Cr) sweep is derived.

Step 3. After VMin is reached, the polarity of the current source changes again to +I and the voltage is measured until VMax is reached. During this step, the forward C-V (Cf) sweep is derived.

Both the forward and reverse C-V curves can be extracted because both the positive and negative current was forced. The derived DUT capacitance (C) is calculated as follows:

$$I = C * \left(\frac{dV}{dt}\right), \text{ therefore } C = I \div \left(\frac{dV}{dt}\right)$$

where: I = forced current (A), V = measured voltage (V), t = time (s), C = derived capacitance (F).

Using the Clarius Software for Force-I QSCV

Tests using the Force-I QSCV method are located in both the Test and Project Libraries that can be found in the Select view by searching for the phrase "force-I QSCV" or just "qscv". Once the tests are found in the Test Library, they can be selected and then added to the project tree. The Test Library includes tests for both a SiC MOSFET (*sic-mosfet-force-i-qscv*) and a SiC MOScap (*sic-moscap-force-i-qscv*). These particular tests can be used with other devices, or a new test can be created by adding a custom test (UTM) to the project tree and using the *force_current_CV* user module found in the *QSCVulib* user library.

The following paragraphs describe the input parameters, output parameters, and analyzing the results of the Force-I QSCV test.

Input Parameters

The input parameters for the Force-I QSCV tests appear in the Configure View of Clarius as shown in **Figure 3**. The user sets both the maximum and minimum test voltages, output current and timing parameters. Open compensation and leakage correction are optional and can also be applied within the Configure View.

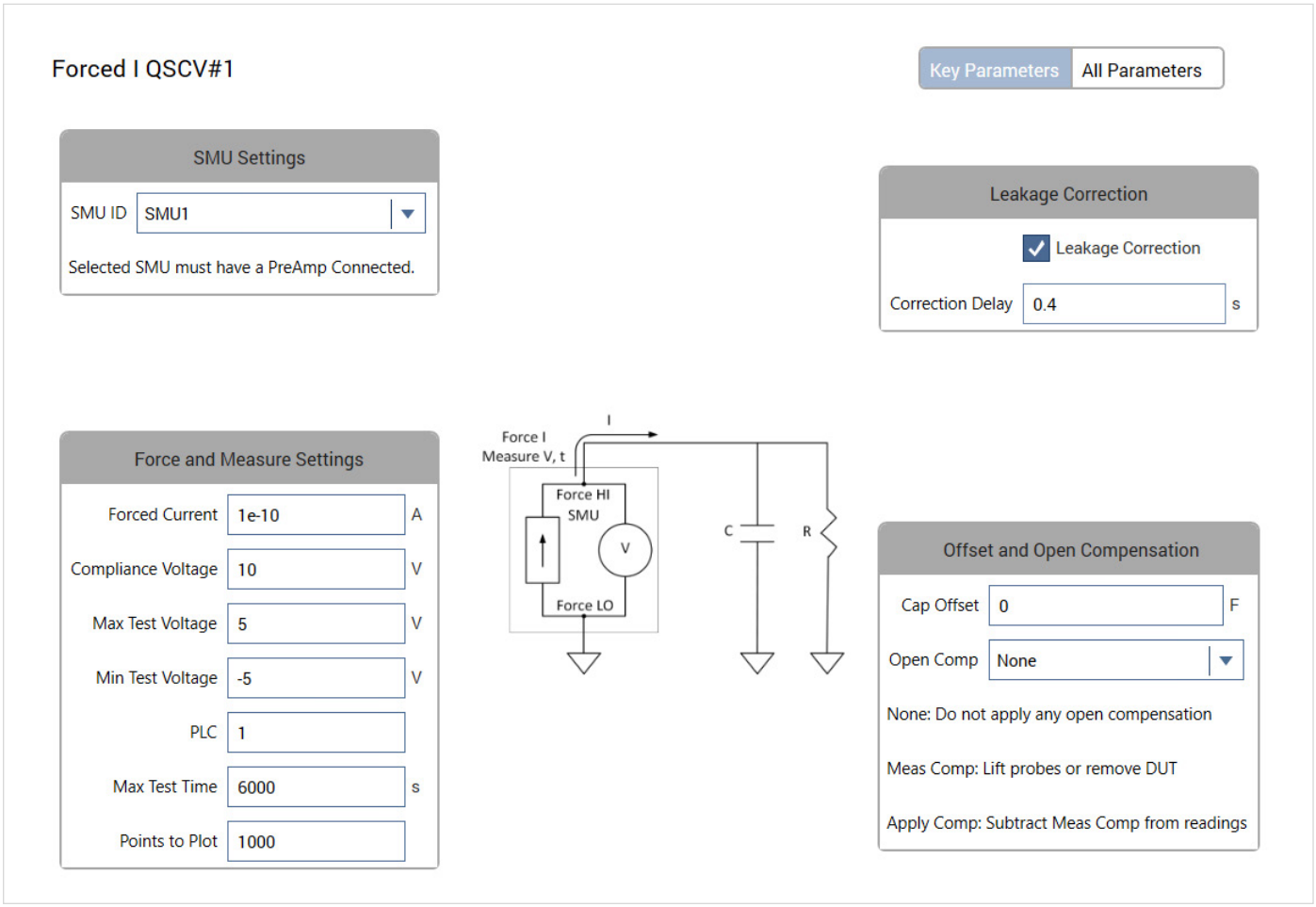


Figure 3. Configure view of the Force-I QSCV test in Clarius.

Table 1 lists all the input parameters with their descriptions and comments.

Table 1. Input parameters of Force-I QSCV test.

Input Parameter	Description	Comments
SMU ID	SMU# to be used in the test.	
Forced Current (A)	DC Current to be applied to DUT.	The lower the capacitance, the lower the test current.
Compliance Voltage (V)	Compliance voltage.	The compliance voltage is reached during the test.
Max Test Voltage (V)	Maximum test voltage to be applied to DUT.	
Min Test Voltage (V)	Minimum test voltage to be applied to DUT.	
Max Test Time (s)	The maximum allowable test time before the test times out.	
PLC	Integration time for both voltage and leakage current measurements.	Set from 0.01 to 10
Leakage Correction (A)	Checkbox for leakage correction.	Current leakage is measured and corrected at each point.
Correction Delay (s)	Settling time allowed after each voltage step. Setting only appears if Leakage Correction enabled.	Leakage is accomplished by forcing voltage, applying step delay, and measuring current.
Cap Offset	The offset to be applied to each capacitance measurement.	
Open Compensation	Choose to not enable Open Compensation (None), to measure the offset (Meas Comp), or apply the acquired offset (Apply Comp).	Open Compensation is a two-part process that is further explained in the paragraphs below.

The following paragraphs contain further information on some of the input parameters.

Forced Current. To choose an appropriate forced current may take some trial and error. The forced current typically is in the hundreds of picoamps to nanoamp range for a SiC MOSFET. The magnitude of the test current should be about a third of the magnitude of the maximum capacitance to be measured. For example, if the maximum capacitance is 2.4E-9 F than the test current should be about 800E-12 A. Using either too low or too high of test current may cause incorrect results.

Too low of test current may take longer for the device to charge up and the measurement time will be longer. Too high of a current will cause the test to reach the compliance voltage only after a few measurement points and return an error to the Sheet in the Analyze view.

The force current for the open compensation should be in the picoamp or less range. Too high of a current will cause the SMU to go into voltage compliance with no sufficient number of measurements collected. Too low of a current will cause very slow measurements.

PLC. The PLC timing setting adjusts the integration time of the measurement and can be set in the range of 0.01 to 10. However, it's best to use PLC values between 1 and 6.

This setting affects the measurement time as well as the voltage step size, which is the voltage difference between the readings. Ideally the step size should be between 50 mV and 100 mV. The voltage step size can be calculated using the DELTA function in the formulator. Increasing the PLC will improve noisy readings at the expense of longer measurement time.

Leakage Correction and Correction Delay. By default, leakage correction is disabled. If it is enabled, current leakage is measured and corrected at each voltage point. Leakage correction is done in three steps:

1. The C-V forward and reverse sweeps are derived using constant current.
2. Then the forward and reverse leakage current is measured at each voltage point returned in the first step.
3. Finally, the measured leakage current is used to correct the returned capacitance values (CrCorr and CfCorr). The leakage current is measured on a fixed current range and can be plotted in real time. Leakage correction uses the following equation for corrected capacitance:

$$C_{corrected} = C_{measured} * (1 - I_{measured}/I_{forced})$$

The corrected reverse capacitance, CrCorr, is plotted against Vr, and the corrected forward capacitance, CfCorr, is plotted against Vf. If the corrected capacitance appears to be noisy, increase the forced current and repeat the test.

The forced current (displacement current) must be higher than the leakage current otherwise the leakage current cannot be corrected. The displacement current is defined as I = C*(dV/dt).

An example of QSCV curves with and without leakage correction are shown in **Figures 4 and 5**. The test was run one time but both the uncorrected and corrected data were generated. **Figure 4** shows the forward (Cf) and reverse (Cr) C-V curves of a leaky SiC power MOSFET.

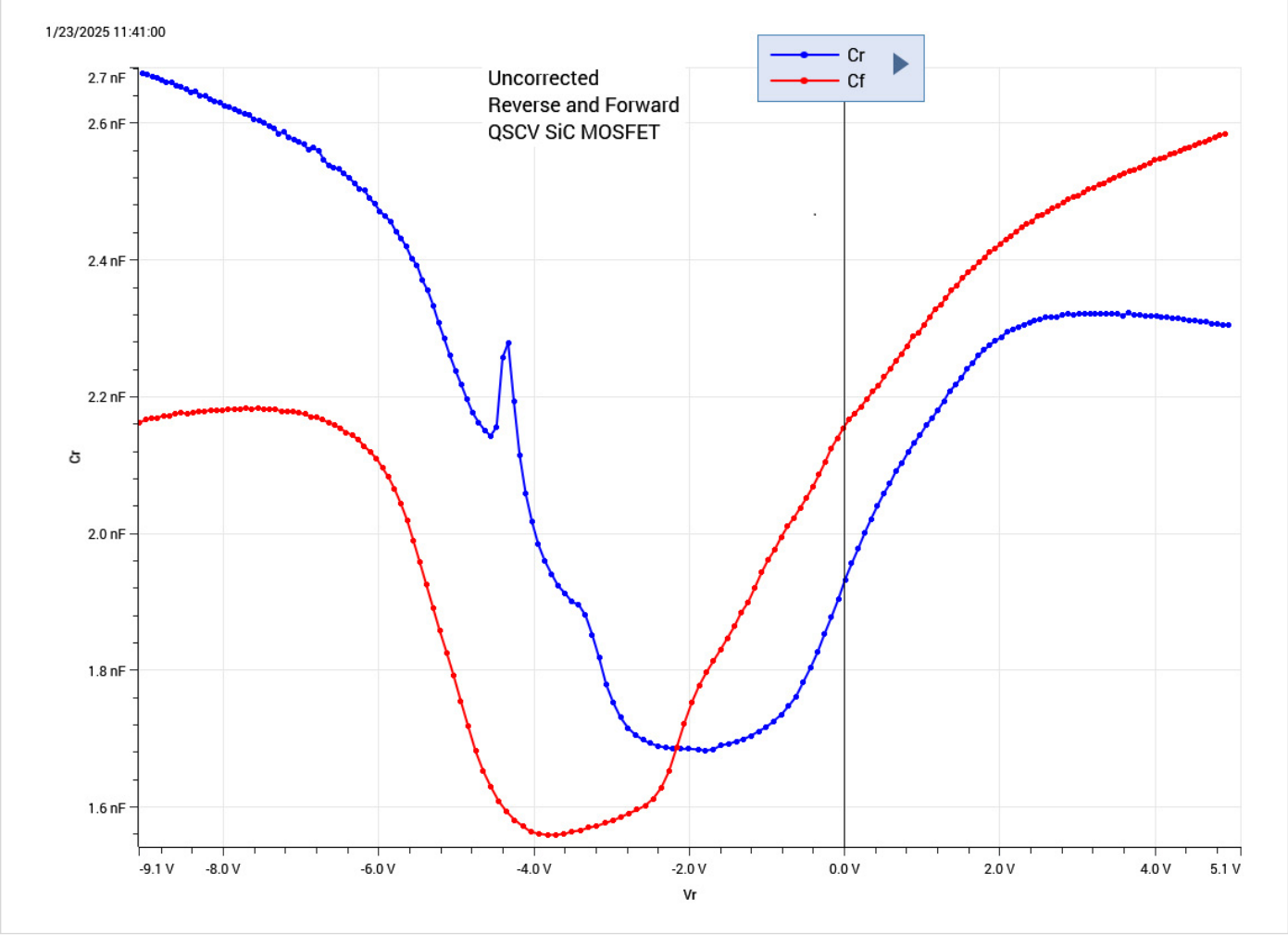


Figure 4. Forward and reverse quasistatic C-V curves of a leaky SiC MOSFET.

Figure 5 shows the results of the corrected forward (CfCorr) and reverse (CrCorr) C-V curves on the leaky device.

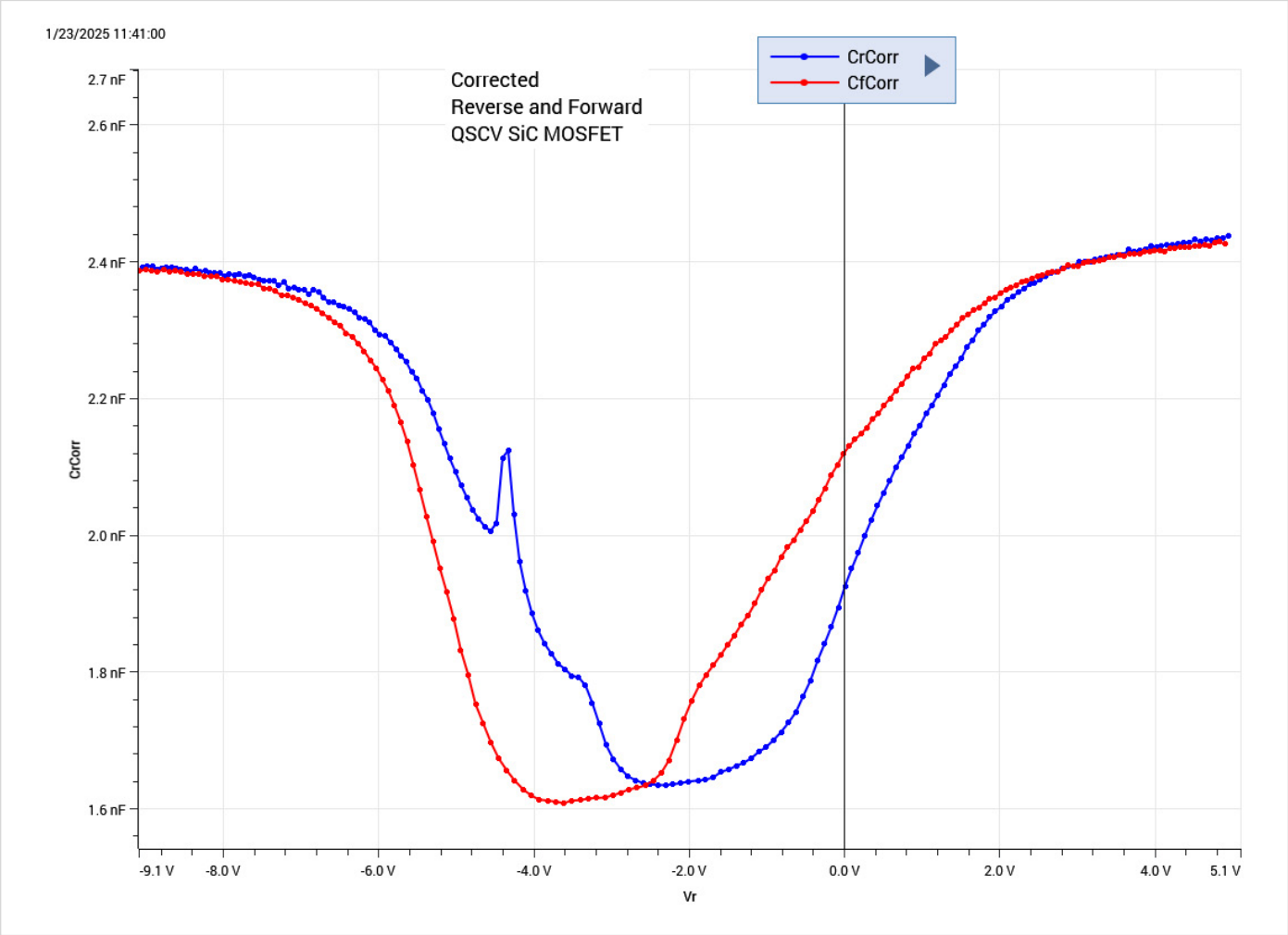


Figure 5. Corrected forward and reverse C-V curves on leaky SiC MOSFET.

Cap Offset and Open Compensation. Both cap offset and open compensation are used to correct for offsets due to capacitances in the test circuit such as cabling, test fixturing or probes. These two options are displayed in the Configure view of the tests as shown in **Figure 6**.

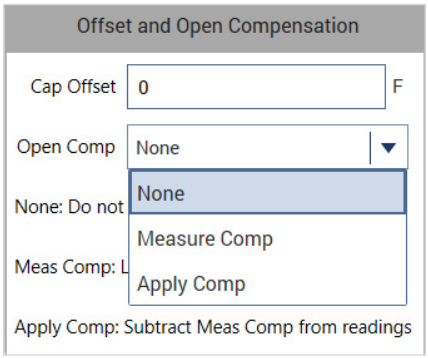


Figure 6. Offset and open compensation window.

By default, cap offset is set to 0 F, but the user can input a capacitance value that will be subtracted from both the forward and reverse capacitance readings.

Open compensation can be set to **None**, **Measure Comp** or **Apply Comp**.

If None is selected, then no open compensation measurements will be written to a file or applied.

If Measure Comp is enabled, the test is run with an open circuit with either the device removed from the test fixture or the probes up. There must be minimum of about 3–5 pF minimum capacitance to correct, otherwise an error (-35) will occur meaning that the SMU is in compliance. Typically, the forced current for an open circuit will be in the 1 E-13 A or less range to avoid the test from going into voltage compliance. Because the test current is so small,

the test will take several minutes to execute and acquire the offset capacitance. The average of the acquired open circuit data is stored in a file and will be subtracted from readings acquired using Apply Comp. The capacitance value that is subtracted is shown in the Sheet as Copen.

Once the test is Run with Measure Comp, then the DUT is connected in the test circuit and the test is Run again with Apply Comp enabled. Make sure to adjust the forced current to an appropriate level for the device. When the test is executed a second time, the average capacitance acquired (Copen) from Meas Comp will be subtracted from subsequent readings.

Analyzing the Results

Once the test is configured with the proper input settings, the test can be executed by selecting Run. When the test is run, a constant current is forced to the DUT as described in Steps 1, 2 and 3 to charge up the device and generate reverse and forward C-V curves.

The Analyze view graph will show the measurements results. The voltage vs. time measurements will appear in real time in the left-side graph and the forward and reverse C-V sweeps will appear in the right-side graph after the voltage measurements are finished.

The data is split into the reverse and forward C-V sweeps to accurately represent the measurements. For the reverse sweep, the reverse voltage (Vr), reverse sweep time (timeR) and reverse capacitance (Cr) are output. In the forward sweep, the reverse voltage (Vf), forward sweep time (timeF) and capacitance (Cf) are output.

Figure 7 shows the results in the Clarius graph view of testing a commercially available SiC power MOSFET using the *sic-mosfet-force-i-qscv* library test. For this test, a test current of 8 e-10 A and 4 PLC were used as test settings. The voltage step size is close to 80 mV using 4 PLC. Notice in the forward and reverse sweeps there is a shift in the voltage and peaks in the curves. Peaks were observed on the forward sweeps on the right side of the curve and on the reverse sweep on the left side of the curve. These shifts are usually attributed to internal device charge movement.

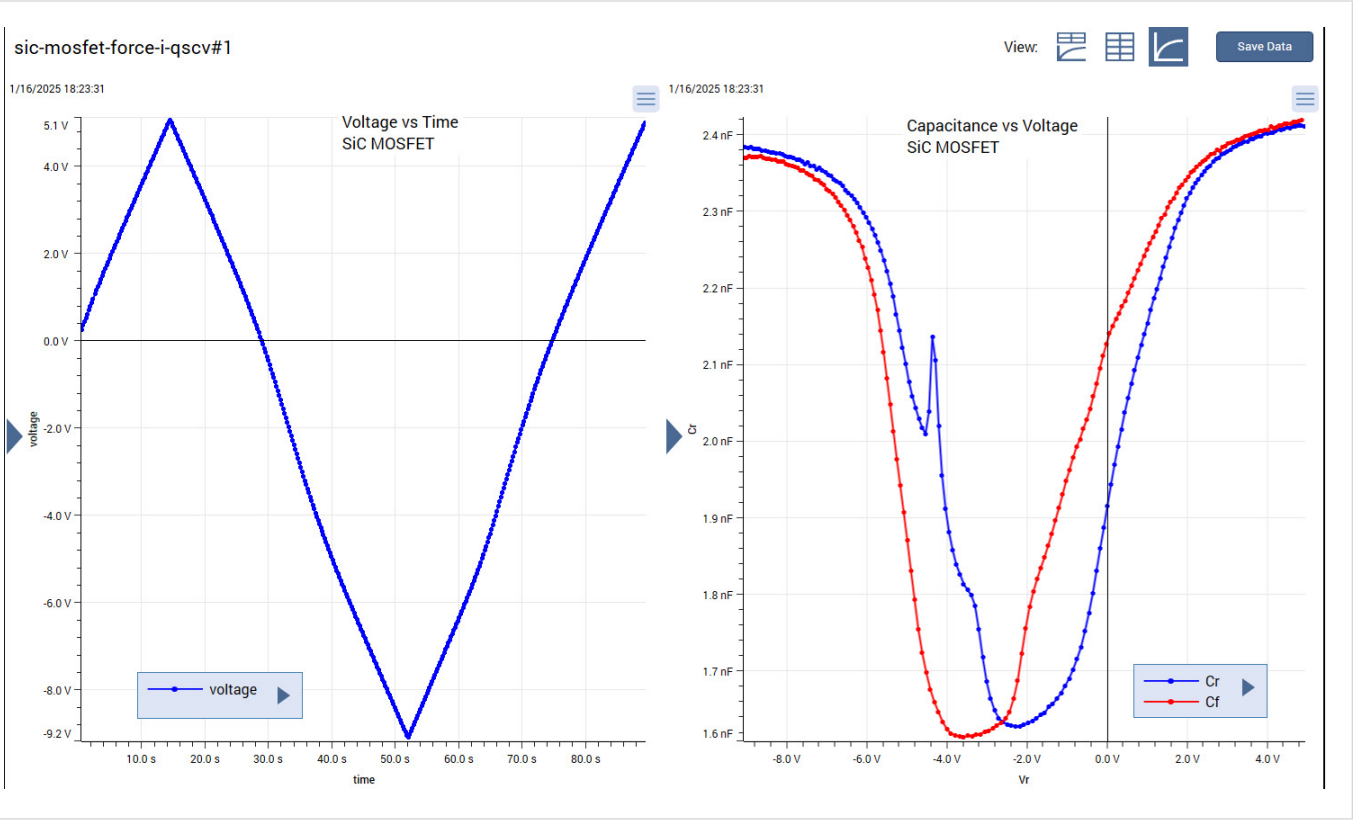


Figure 7. Voltage vs. time (left) and reverse and forward C-V graphs (right) of a SiC MOSFET.

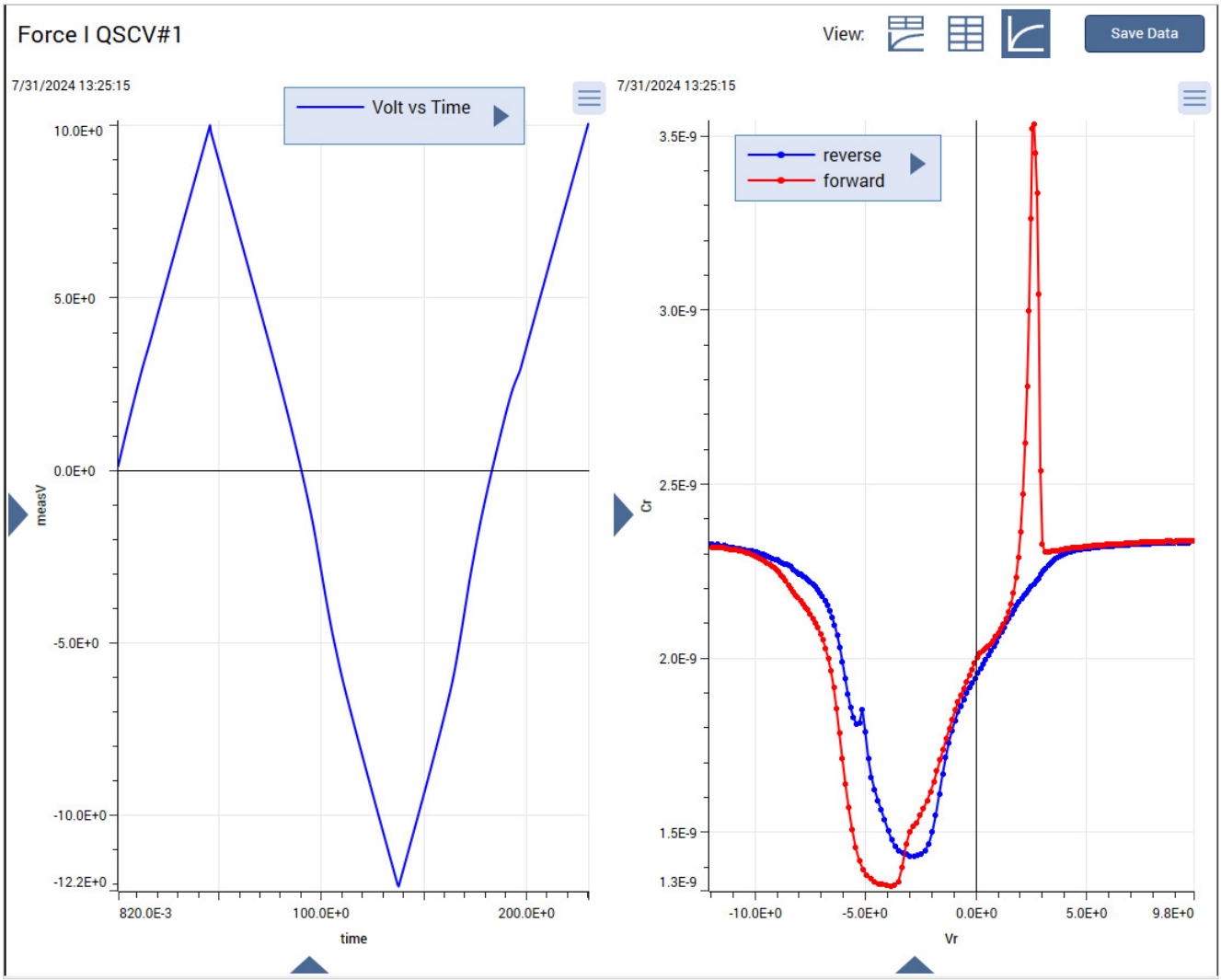


Figure 8. Forward and reverse quasistatic C-V sweeps on SiC MOSFET.

Example quasistatic C-V curves from a different commercially available SiC MOSFET are shown in **Figure 8**. In this case, the forward (red) curve has a "mobile ion" like peak that is not exhibited in the reverse sweep. For this test, the input parameters were set as follows: test current 5 e-10 A, 8 PLC, max voltage 10 V, min voltage -12 V, compliance 20 V.

In addition to looking at the data in the Graph tool, several parameters are returned to the Sheet in the Analyze View. These output parameters are listed in the following tables and are separated in the order shown in the Sheet as well as grouped into these categories: primary output parameters, reverse output parameters, forward output parameters, parameters used for DIT extraction, and miscellaneous parameters.

Table 2. Primary output parameters.

Output Parameter	Description	Comments
Voltage (V)	Voltage measured as a function of time across the device. Voltage = Vg.	Check to make sure the step size is between about 50 mV to 100 mV.
Vs (V)	Surface Potential defined as Vs=Vg-(Q/Cox) where Vg=Voltage	
charge (C)	Charge is defined as Q=∑I*dt supplied to the device (coulombs)	
time (s)	Time at each point	

Table 3. Reverse output parameters

Output Parameter	Description	Comments
Vr (V)	Reverse voltage from Step 2.	
Vrs (V)	Calculated surface potential for reverse voltage defined in Step 2.	Vsr=Vg-(Q/Cox), where Vg=Voltage
timeR (s)	Time array for the reverse sweep	
Cr (F)	Capacitance from reverse voltage sweep	
Ir (A)	Measured leakage current.	Leakage current is measured by forcing voltage at each voltage step in the Cr sweep and then measuring the current.
CrCorr (F)	Capacitance corrected to compensate for leakage current.	CrCorr = Cox(1-Ir/Iforce) where Iforce = Forced Current

Table 4. Forward output parameters.

Output Parameter	Description	Comments
Vf (V)	Forward voltage from Step 2.	
Vfs (V)	Calculated surface potential for forward voltage defined in Step 2.	Vfs=Vg-(Q/Cox), where Vg=Voltage
timeF (s)	Time array for the forward sweep.	
Cf (F)	Capacitance from forward voltage sweep.	
If (A)	Measured leakage current.	Leakage current is measured by forcing voltage at each voltage step in the Cf sweep and then measuring the current after the input Step Delay.
CfCorr (F)	Capacitance corrected to compensate for leakage current	CfCorr = Cox(1-If/Iforce) where Iforce = Forced Current

Table 5. Parameters used for DIT extraction.

Output Parameter	Description	Comments
CrDut (F)	Interpolated reverse capacitance.	
CfDut (F)	Interpolated forward capacitance.	
CrOnly (F)	Interpolated reverse capacitance with Cox removed.	
CfOnly (F)	Interpolated forward capacitance with Cox removed.	
Cdut_diff (F)	An array of values that represent the difference between the forward (CfOnly) and reverse (CrOnly) DUT capacitance values.	Plot with Vdut_diff.
Vdut_diff (V)	An array of differential voltage values that correspond to the surface potential	Plot with Cdut_diff.

Table 6. Miscellaneous output parameters.

Output Parameter	Description	Comments
Cox (F)	Maximum capacitance of both the Cr and Cf data.	
Copen (F)	Value used for open compensation	Copen is always returned even though this value doesn't get written to the file unless Meas Comp is selected.

Optimizing the Force-I QSCV Method

Minimum Capacitance. The minimum capacitance that can be measured is between 10–20 pF. This method is recommended for SiC devices that typically have capacitances in the nF range.

Electrostatically Shield the Device. Because this method involves detecting very small charges, it is important to electrostatically shield the device under test to avoid noisy measurements.

Voltage Step Size. The voltage step size should be between 50–100 mV for optimal results. The voltage step size can be adjusted by changing the PLC. The voltage step size can be measured using the DELTA function in the Formulator of the measured "voltage" in the Sheet.

Forced Current. Choosing the appropriate test current may take some trial and error. Too low of current will cause long test times. Too high of current will cause the test to reach compliance.

Open Compensation. In most cases of measuring QSCV on SiC devices, open compensation will not be necessary because cable and test fixturing capacitance (10 s of pF) is usually much smaller than the DUT capacitance (nF).

Force-I QSCV vs. Keithley 595 Quasistatic C-V Meter

The Keithley 595 Quasistatic C-V Meter, now obsolete, was used to make quasistatic C-V measurements on semiconductor devices. The 595 used a feedback charge method to measure capacitance. This method measured coulombs to derive the capacitance unlike most methods available today that measure current.

Comparisons were made between forward and reverse C-V curves taken with the 595 and the Force-I QSCV method on both SiC MOScaps on a wafer and commercially available SiC MOSFETs. Results of the forward and reverse quasistatic C-V curves taken on a SiC MOScap are shown in **Figure 9**. Notice the curves from the two methods overlap.

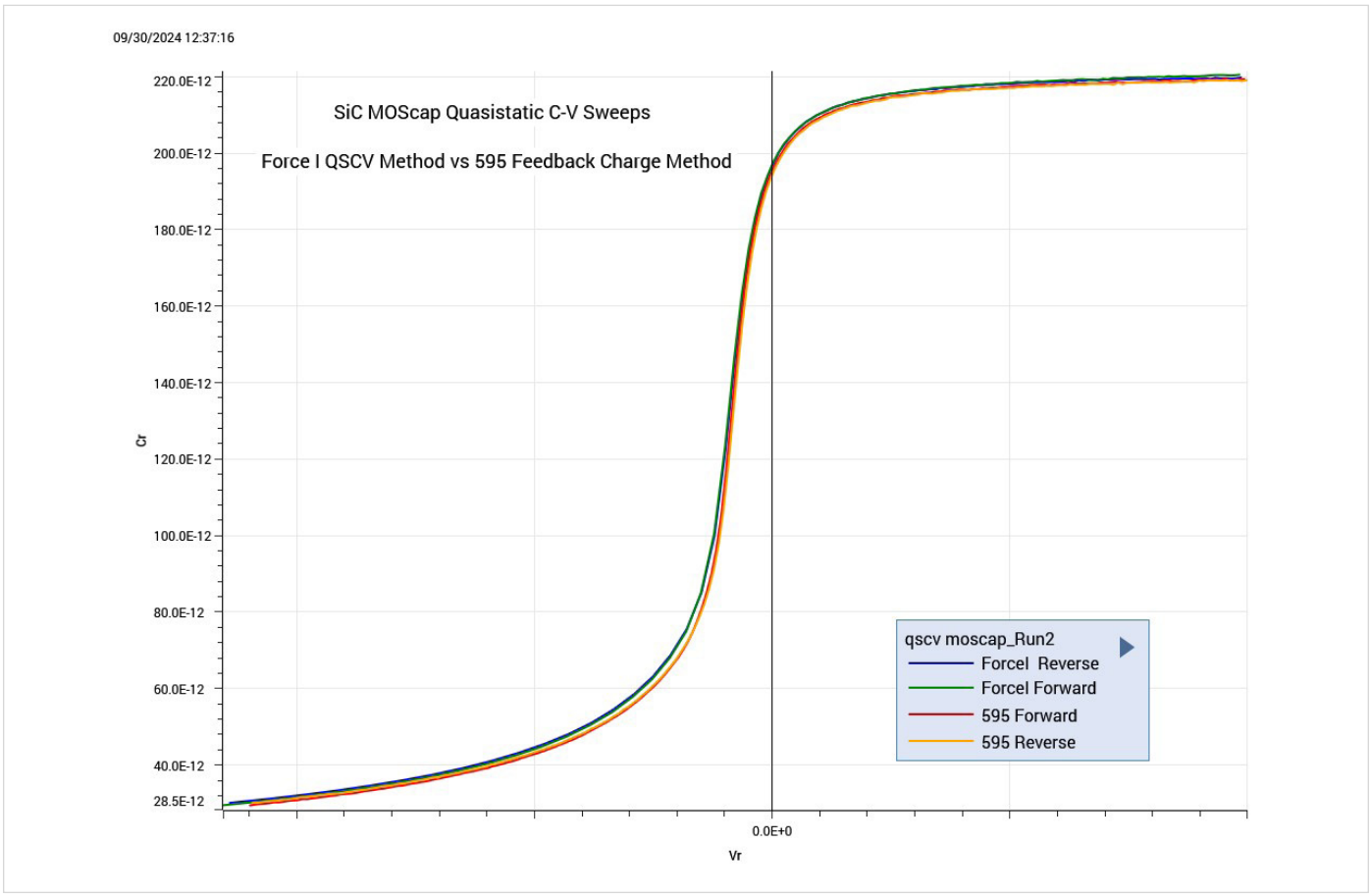


Figure 9. 595 and Force-I QSCV SiC MOScap forward and reverse quasistatic C-V curves.

Figure 10 shows graphs using both methods taken on a packaged SiC MOSFET. Notice the Force-I QSCV curves are less noisy than the 595 data, but in general, the curves correlate nicely.

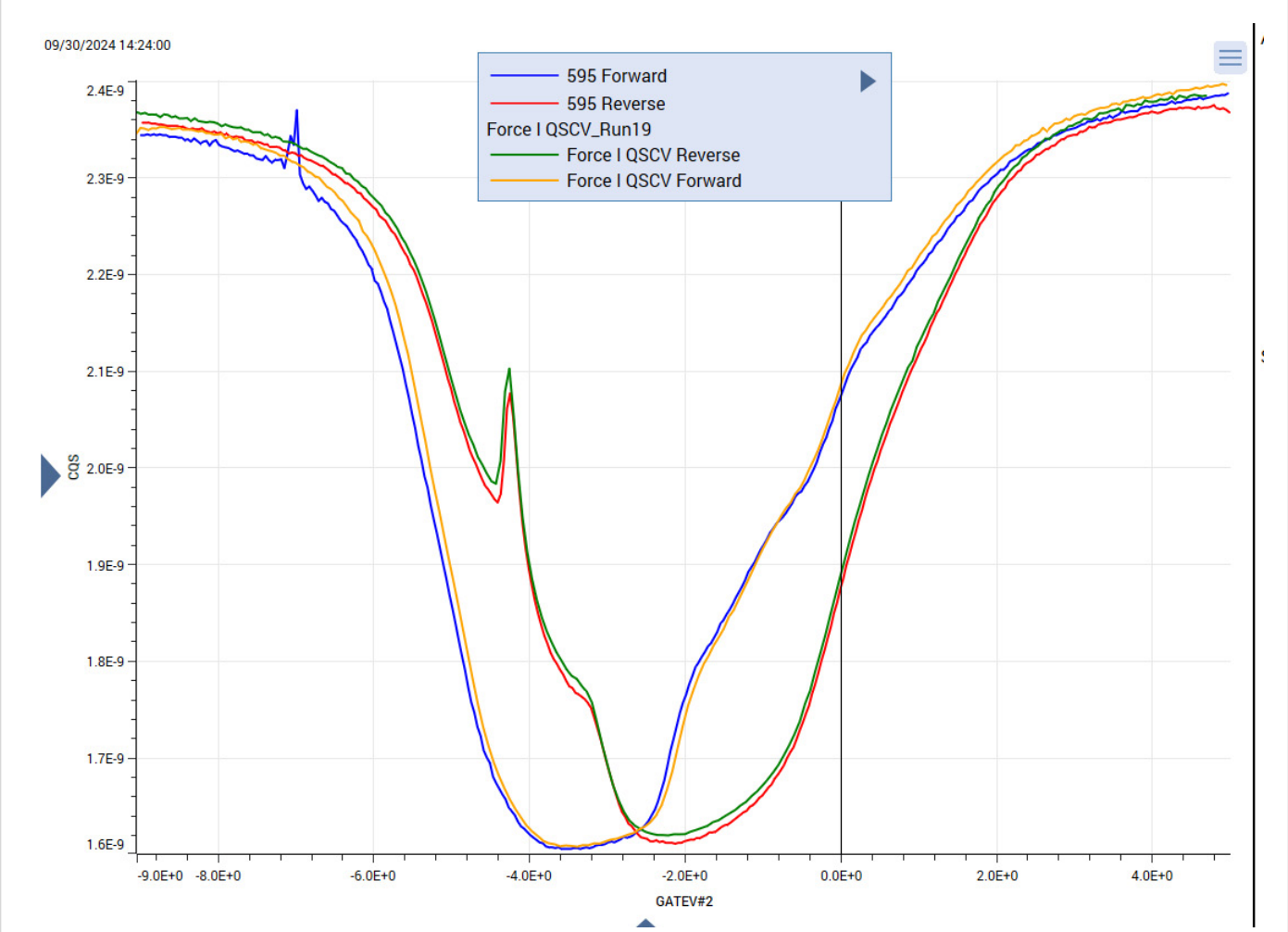


Figure 10. Both 595 and Force-I QSCV forward and reverse curves on SiC MOSFET.

Force-I QSCV vs. High Frequency C-V

Comparisons of C-V curves taken with the Force-I QSCV method and high frequency AC measurements (using the 4215-CVU Capacitance Voltage Unit) were also observed. The results are shown in **Figure 11**. The CVU data (green curve) encompassed both the forward and reverse quasistatic curves from both the 595 and the Force-I QSCV methods. The high frequency CVU data did not show any "peaks" in the curve.

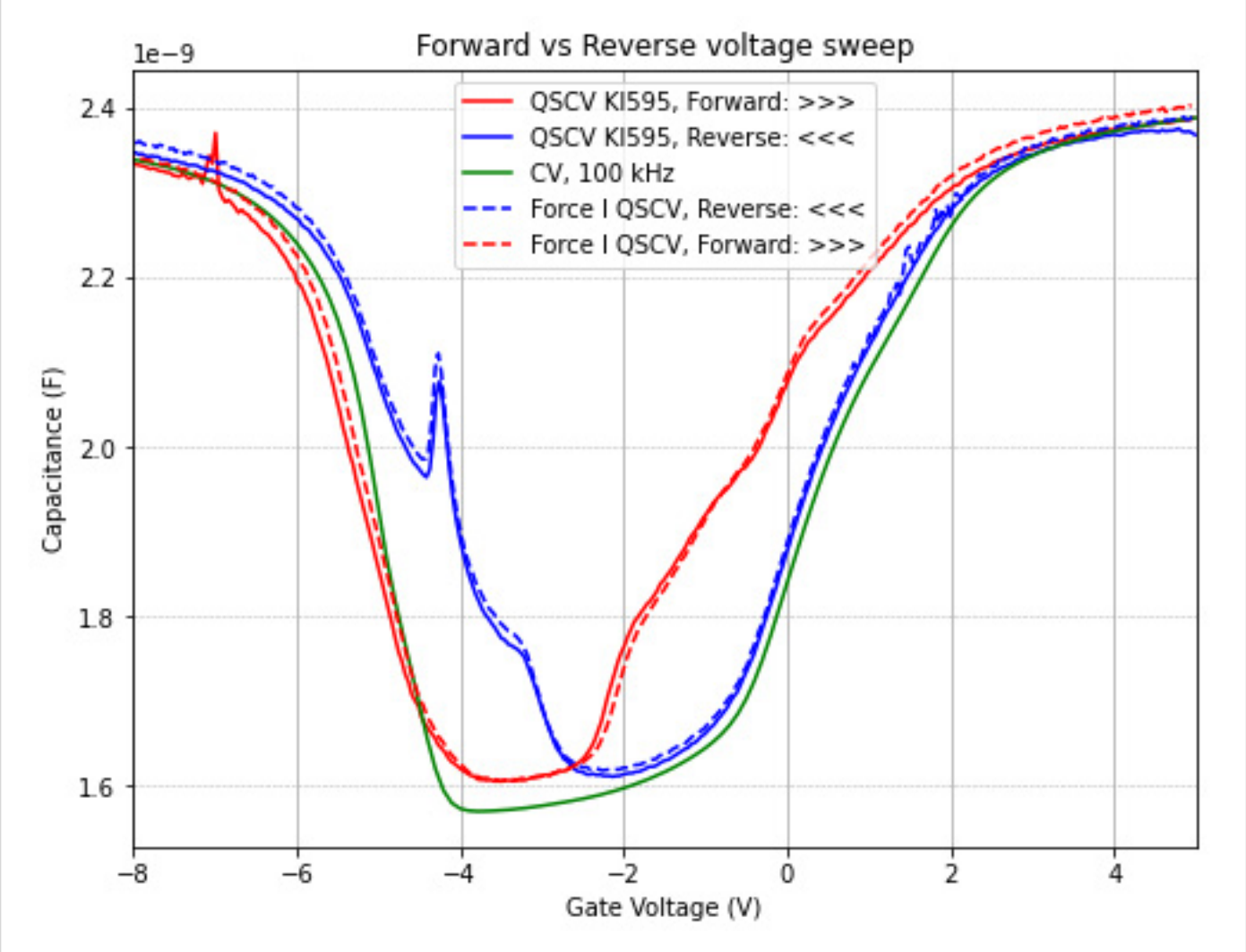


Figure 11. High frequency and quasistatic C-V sweeps on packaged SiC MOSFET.

C-V Measurements and Interface Trap Density on SiC MOS Devices

At the time of this writing (March 2025), we are in the process of verifying that the suggested interface trap density (DIT) calculations on both SiC MOSFETs and MOScaps using the Force-I QSCV method correlate with other known techniques, such as the comparison of combined low and high frequency capacitance measurements. The following paragraphs discuss these derivations.

SiC MOSFETs

Traditionally, the interface trapped charge of a silicon MOS cap was extracted from the capacitance difference of a low frequency (quasistatic) C-Vg curve and a high frequency (AC) C-Vg curve. We've learned that to observe internal charges of a SiC MOSFET, the forward and reverse quasistatic C-Vg sweeps can be used to extract this charge.

Because SiC MOSFETs have significantly more internal charges than traditional Si devices, the measured capacitance needs to be plotted against the surface potential (Vs) as opposed to the gate voltage (Vg) for calculations of trapped charges. Because charge is measured, the interface potential can be calculated. This enables the capacitance to be characterized as a function of the interface potential. In standard techniques, it's difficult to extract the interface potential because it's difficult or impossible to measure the oxide charge at a high frequency. Therefore, comparisons are usually made as a function of the gate voltage and not the interface potential.

The technique for deriving this interface trap capacitance can be summarized into five steps:

1. Generate forward (Cf) and reverse (Cr) quasistatic capacitance vs. gate voltage (Vg) curves on a SiC MOSFET using the Force-I QSCV method.
2. Derive surface potential (Vs) arrays for both forward and reverse sweeps.
3. Interpolate the forward capacitance (CfDut) and reverse capacitance (CrDut) at each surface potential point.
4. Subtract the oxide capacitance (Cox) from the forward (CfDut) and reverse (CrDut) measurements.
5. Calculate the capacitance (CIT) and interface trap density (DIT) due to trapped charge from the difference of the forward and reverse curves as a function of the surface potential.

These five steps are further explained in the following paragraphs:

Step 1. Generate Forward and Reverse Quasistatic C-V Curves.

Generate forward (Cf) and reverse (Cr) quasistatic capacitance vs. gate voltage (Vg) curves on a SiC MOSFET using the Force-I QSCV method.

From the forward and reverse C-V sweeps there is both a shift in the voltage between the two curves as well as "peaks" and smaller curve features (see Figures 4 and 5). We believe both the voltage shift and "peaks" are a result of internal devices charges such as trapped charges or mobile ion charge, or charges related to the device structure. Interestingly, when a high frequency C-V sweep is generated, the voltage shift and peaks are not observed.

Step 2. Derive Surface Potential (Vs) Arrays for both Forward and Reverse Sweeps

The capacitances of forward and reverse voltage sweeps of a MOS device are usually compared at the same gate voltage (Vg). Because SiC MOSFETs have significant internal charges, we compared the forward and reverse quasistatic curves as a function of the surface potential (Vs) instead. Using Vs corrects for the "shifts" seen in the gate voltage between the forward and reverse curves and allows for the curves to be compared. Accurately measured charge allowed us to correct for the voltage drop across the gate oxide to extract Vs.

Figure 12 shows the SMU applying a constant current to a SiC MOS DUT as well as the voltages, Vg and Vs. The voltage at the gate terminal of the device is Vg. The voltage at the SiC/SiO2 interface is the surface potential (Vs) and is represented by the equation:

$$Vs = Vg - Vox, \text{ where } Vox = Q/Cox$$

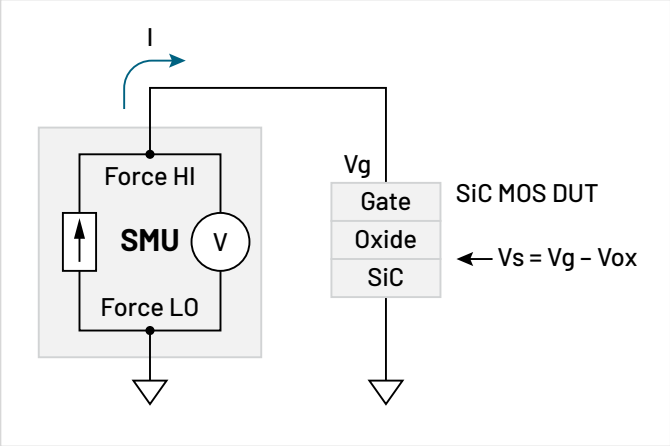


Figure 12. A SMU connected to SIC MOS Dut with circuit potentials.

First, the reverse and forward capacitance arrays (Cr and Cf) are analyzed to find the maximum value from either array. The maximum capacitance is defined as Cox, or oxide capacitance.

Then, from each gate voltage (Vg), the surface potential Vs is calculated using the oxide capacitance (Cox) and calculated charge (Q):

$$Vs = Vg - \frac{Q}{Cox}$$

Finally, the surface potential is split into two separate arrays for both sweeps. The output parameter, VsR, represents the reverse sweep surface potential, and VsF represents the forward sweep surface potential.

Step 3. Interpolate the forward capacitance (CfDut) and reverse capacitance (CrDut) at each surface potential point.

The forward and reverse data sets were collected at different gate voltages, but they need to be compared at the same surface potential. To do this, a linear interpolation algorithm is used.

The following process is used for linear interpolation:

a. Determine the number of voltage step points but using the following equation:

$$\Delta V = \frac{Vmax - Vmin}{(points\ to\ plot) - 1}$$

b. Run the linear interpolation twice, once for the reverse sweep and another for the forward sweep to extract the interpolated capacitance points. The forward and reverse interpolated capacitance arrays are CrDut and CfDut.

Step 4. Subtract the Oxide Capacitance from the Forward (CfDut) and Reverse (CrDut) Measurements.

Subtract and maximum capacitance (Cox) from all CrDut and CfDut values. To do this, the linear interpolation algorithm is run using the reverse and forward voltage surface potential values, VsR and VsF. The forward and reverse interpolated capacitance arrays are calculated, and in each function, the Cox value is removed at each point, using the following two equations:

$$Cf\ Only = \frac{1}{\frac{1}{Cf\ Dut} - \frac{1}{Cox}}$$

$$Cr\ Only = \frac{1}{\frac{1}{Cr\ Dut} - \frac{1}{Cox}}$$

Figure 13 shows both the forward and reverse capacitance curves, CfDut and CrDut, plotted as a function of interface voltage instead of gate voltage.

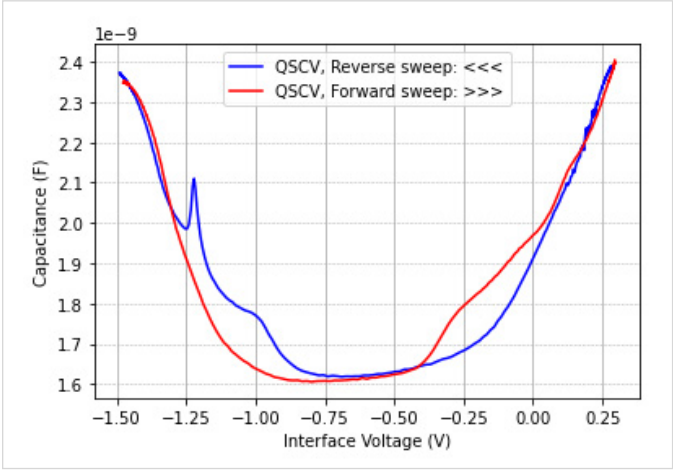


Figure 13. Forward and reverse capacitance curves as a function of Vs.

In **Figure 14**, with Cox removed, CrOnly and CfOnly are plotted as a function of interface voltage, now in a logarithmic scale.

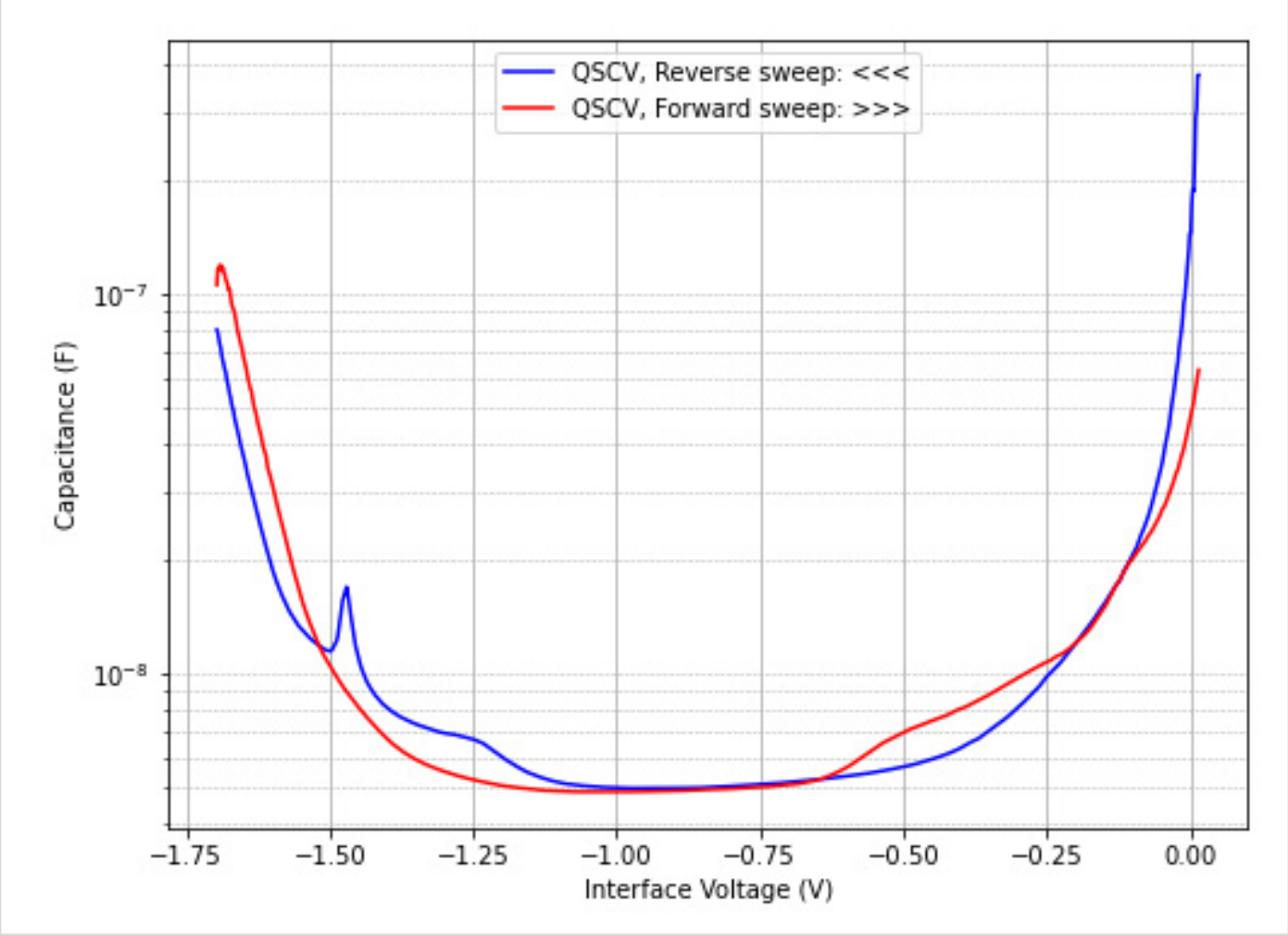


Figure 14. Cf and Cr curves with Cox removed as a function of Vs.

Step 5. Calculate the interface trapped capacitance (CIT) and density (DIT)

Calculate the capacitance (CIT) due to trapped charge from the difference of the corrected forward and reverse curves as a function of the surface potential.

$$CIT = [C_{Fonly}(V_s) - C_{Ronly}(V_s)] / \text{ gate area}$$

The interface trap density (DIT) is also derived using the following equation:

$$DIT = [C_{Fonly}(V_s) - C_{Ronly}(V_s)] / (\text{gate area} * q)$$

Figure 15 shows a plot of the interface trap density (DIT) as a function of surface potential (Vs).

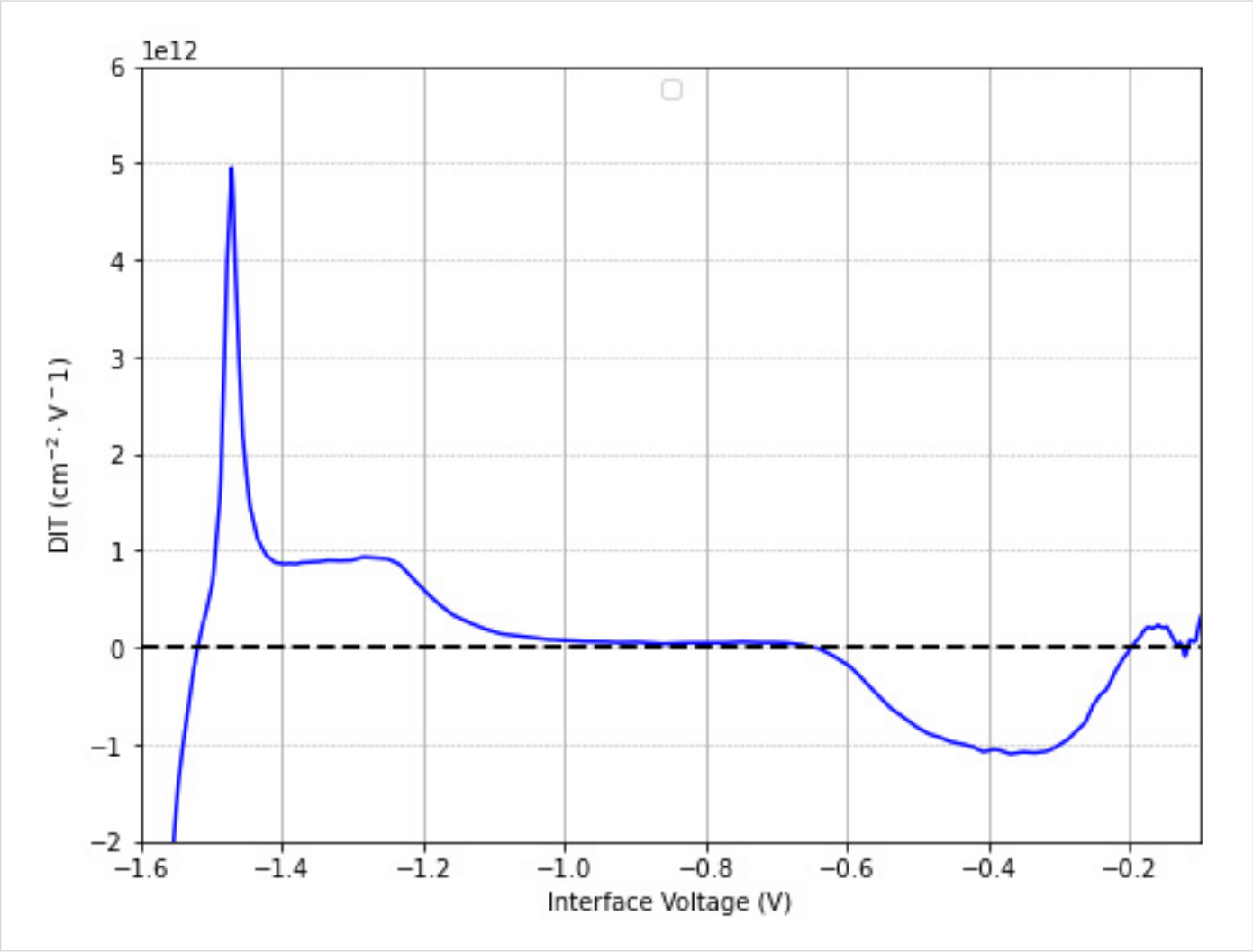


Figure 15. Plotted difference between the interpolated forward and reverse capacitances vs. interface voltage (Vs).

SiC MOScap

For interface trap density (DIT) measurements on a MOScap, a combination of both high and low frequency measurements is used. When generating both high frequency and quasistatic C-V curves, make sure the voltage step size is much smaller than the voltage difference between the two curves. The voltage step size can be reduced by decreasing the PLC value.

We are still investigating the DIT extraction of both SiC MOScaps and MOSFETs using the Force-I QSCV technique.

Conclusion

The Force-I QSCV technique enables quasistatic C-V measurements on SiC MOS devices. This method acquires two sets of data from forward and reverse sweeps as well as voltage vs. time data obtained by forcing positive and negative currents. With the total charge known, this method allows for the extraction of capacitance and charge at the semiconductor interface. Differential analysis of forward and reverse sweeps enables direct extraction of the density of interface traps (DIT).

Appendix 1. Error Codes

These error codes in **Table 7** appear in the first column, first row of the Sheet in the Analyze view after the test is executed. Below is a description of the error and provide help on what to do.

Table 7. Error codes for the *force_current_cv* user module.

Error Codes	Description
0	OK.
-20	The forced current is less than the minimum current of 5e-14 Amps. Increase the forced current.
-21	Min Test Voltage (vLow) or Max Test Voltage (vHigh) exceeds the absolute voltage limit (vLimit). Decrease the Min or Max Test Voltage or increase the compliance voltage.
-22	Max Test Voltage (vHigh) is smaller than Min Test Voltage (vLow). Increase the Max Test Voltage or decrease the Min Test Voltage.
-23	Polarity of the Forced Current (Iforce) is not consistent with polarity of Min Test Voltage (vLow) and Max Test Voltage (vHigh). Change the polarity of the forced current.
-30	Selected SMU is not present in the system.
-35	In the initial sweep the absolute measured voltage is greater than the absolute voltage limit. Increase the compliance voltage. The measured capacitance is too small to measure. The minimum measurable capacitance is about 10-20pF.
-37	Internal memory values could not be allocated. Please check system memory usage.
-40	The initial sweep count is greater than the maximum number of steps. Increase the forced current, PLC, or maximum number of steps.
-50	Test time during the initial sweep exceeded the maximum time. Increase the max test time or forced current.
-55	Not enough initial points to continue the test. Decrease the forced current. Minimum capacitance is too small.
-60	The reverse sweep count exceeded the maximum number of steps. Increase the forced current, PLC, or maximum number of steps.
-70	Test time during the reverse sweep exceeded the maximum time. Increase the max test time or forced current.
-76	In the reverse sweep the absolute measured voltage is greater than the absolute voltage limit. Increase the compliance voltage.
-90	The forward sweep count exceeded the maximum number of steps. Increase the forced current, PLC, or maximum number of steps.
-100	Test time during the forward sweep exceeded the maximum time. Increase the max test time or forced current.
-104	In the forward sweep the absolute measured voltage is greater than the absolute voltage limit. Increase the compliance voltage.
-110	Error during writing the offset to the filesystem. Check write access to C:\\S4200\\kiuser\\coffset.csv

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