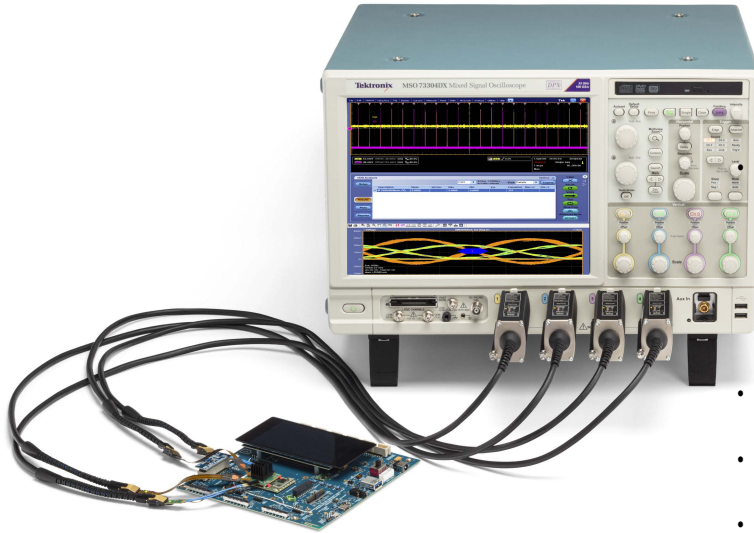


LPDDR5-5X Memory Interface Electrical Verification and Debug

Opt. LPDDR5SYS and 7-CMLPDDR5SYS – System Level Transmitter Tests Datasheet



DDR (Dual Data Rate) is a dominant and fast-growing memory technology. It offers high data transfer rates required for computing applications, from consumer products to the most powerful servers. The high speed of these signals requires high-performance measurement tools. Tektronix TekExpress DDR Tx is an automated test application used to validate and debug the LPDDR5-5X designs of the DUT as per the JEDEC specifications. The solution enables you to achieve new levels of productivity, efficiency, and measurement reliability.

Key features

- Supports 319 measurements of LPDDR5-5X System Transmitter Tests as per LPDDR5 JEDEC specification:
 - 15 Clock Differential measurements
 - 30 Clock Single Ended measurements
 - 15 Clock Single Ended Positive Leg measurements
 - 18 Write Clock Differential measurements
 - 33 Write Clock Single Ended measurements
 - 18 Write Clock Single Ended Positive Leg measurements
 - 18 Write Clock Single Ended Negative Leg measurements
 - 27 Write Burst Differential measurements
 - 19 Write Burst Single Ended measurements
 - 23 Write Burst Single Ended Positive Leg measurements
 - 23 Write Burst Single Ended Negative Leg measurements
 - 11 Read Burst Differential measurements

- 12 Read Burst Single Ended measurements
- 15 Read Burst Single Ended Positive Leg measurements
- 15 Read Burst Single Ended Negative Leg measurements
- 15 CA Rx Specification measurements
- 12 CS Rx Specification measurements

User-Defined Acquisition (UDA) mode for Clock, Write Clock, CA, CS, Data Strobe, and data for both Write and Read traffic (or bursts).

UDA: TekExpress DDR Tx for LPDDR5-5X Transmitter Solution puts control back where it should be, with the user. User defined acquisition mode allows you to run LPDDR5-5X JEDEC compliance measurements by customizing scope settings like sample rate, record length, bandwidth, and more

- De-embedding support for Clock, Write Clock, CA, CS, Data Strobe, and data for both Write and Read traffic (or bursts)
- Number of UIs support for Clock, Write Clock, Read/Write data, CA and CS measurements
- Multi-Run feature is applicable for all tests
- Save worst case waveform in known/TekExpress sessions
- Retain Vertical Scale settings supported during acquisition
- User-friendly measurement configurations
- Test report to reflect all the statistics of the measurement
- User can select the source and the channel in the acquisition panel
- Multiple Burst Detection Methods are supported:
 - Read and Write
 - Write Only
 - Read Only
 - Visual Search¹
- Hexagon shape mask and margin analysis for Write Data, CA, CS Eye measurement
- Custom Data Rate support upto 15000MT/s
- Single Ended mode support

Applications

Tektronix provides the most comprehensive solution to serve the needs of the engineers designing DDR silicon for server, computer, graphics systems, mobile, embedded systems, and for those who are validating the physical-layer compliance of DDR Memory Compliance Test Specification.

The Tektronix option LPDDR5SYS (TekExpress DDR Tx) includes compliance and debug solution for the following:

- DRAM components

¹ This feature is supported only for MSO/DPO70000 DX/SX oscilloscope models (opt. LPDDR5SYS)

- System boards
- Embedded systems
- Mobile
- Automotive
- Internet of things (IoT)

The Tektronix option LPDDR5SYS is compatible with the following Tektronix oscilloscope models:

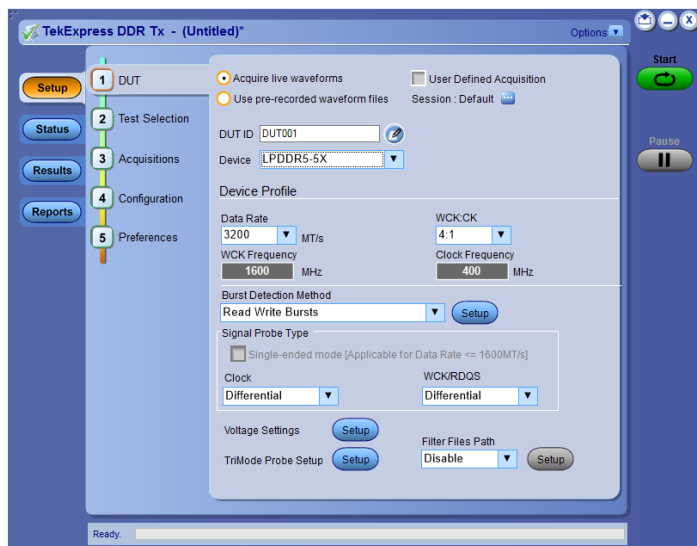
- 7 Series scope, model DPO714AX at 16 GHz, 20 GHz, and 25 GHz
- MS071604DX, MS072004DX, MS072304DX, MS072504DX, and MS073304DX
- DPO73304DX
- Non-ATI channels of DPO75002SX, DPO75902SX, DPO7702SX, DPS75004SX, DPS75904SX, DPS77004SX and DPO73304SX

The above-mentioned Tektronix oscilloscopes are designed to meet the challenges of the next generation memory standards and provide the industry's leading vertical noise performance with the highest number of effective bits (ENOB) and flattest frequency response for oscilloscopes in their class.

LPDDR5-5X system level tests

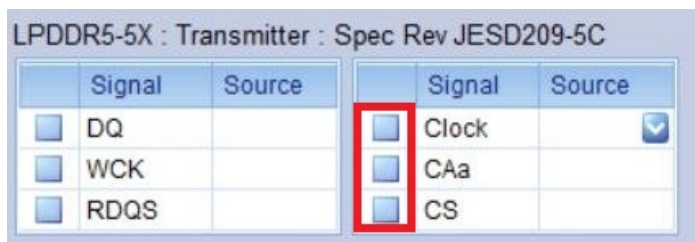
The Tektronix TekExpress DDR Tx solution reduces the effort and accelerates the compliance testing for DDR systems and devices with several unique and innovative capabilities.

The TekExpress DDR Tx application provides a simple, step-by-step, and easy-to-use interface to speed up the testing process. Users can select the memory technology of interest in Device, Data Rate, Burst Detection Method, select the probing configuration used for Clock, and strobe in the Setup DUT panel. Perform the test selection in the next step as per the measurement group (Clock, Command Address, Data Strobe, and Data for both Read and Write traffic (or bursts)) and individual measurements within the group provide different methods of Burst detection.



TekExpress DDR Tx – application launch screen for LPDDR5-5X

The TekExpress DDR Tx application comes with a unique feature to select or deselect the signal. Once the signal is selected in the acquisition panel, the user can select the signal source connected to the oscilloscope.



Acquisition panel – signal source selection for LPDDR5-5X

De-embed filters

Easily de-embed the interposer and the probe effects by applying suitable de-embed filters within the LPDDR5-5X standard.



De-embed filters for LPDDR5-5X

Comprehensive measurements

The options LPDDR5SYS and 7-CMLPDDR5SYS adds a long list of JEDEC specific measurements for LPDDR5-5X memory standards. The TekExpress DDR Tx application covers Electrical measurements, Timing measurements, and Eye Diagram measurements as per the JEDEC standards.

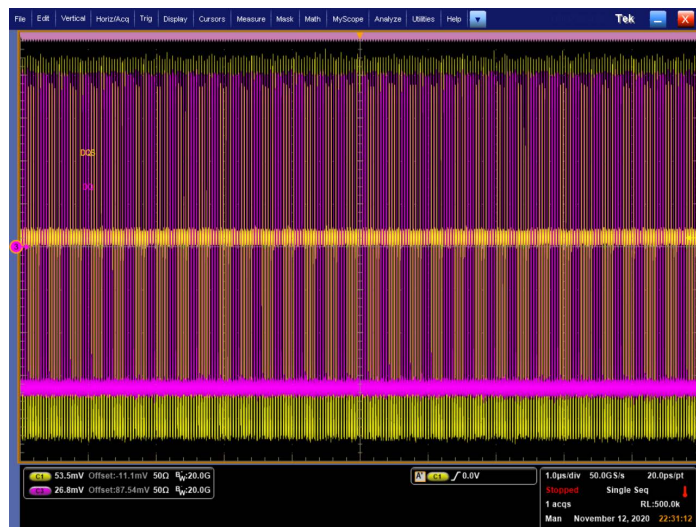
Automated Read and Write Burst detection

The TekExpress DDR Tx provides different ways to detect the burst cycles that are used to perform measurements:

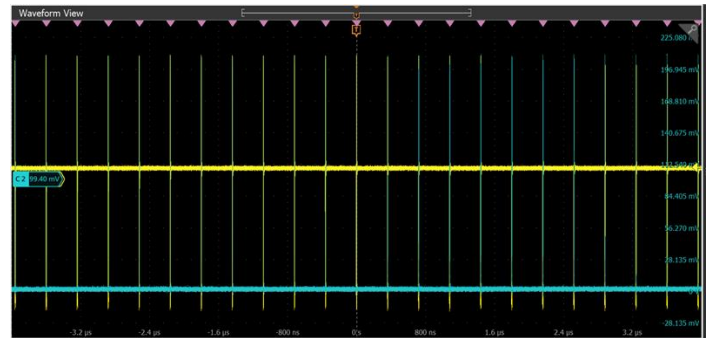
- Read Write Bursts – when the DUT traffic is configured to send both Read and Write bursts then this method is used for burst detection.
- Write Only – when the DUT traffic is configured to send all Write Bursts then this method is used for burst detection.
- Read Only – when the DUT traffic is configured to send all Read Bursts then this method is used for burst detection.
- Visual Search¹ – defining Visual Trigger areas to identify and gate area of interest for measurements

Burst Detection Method
Read Write Bursts
Read Write Bursts
Write Only Bursts
Read Only Bursts
Visual Search

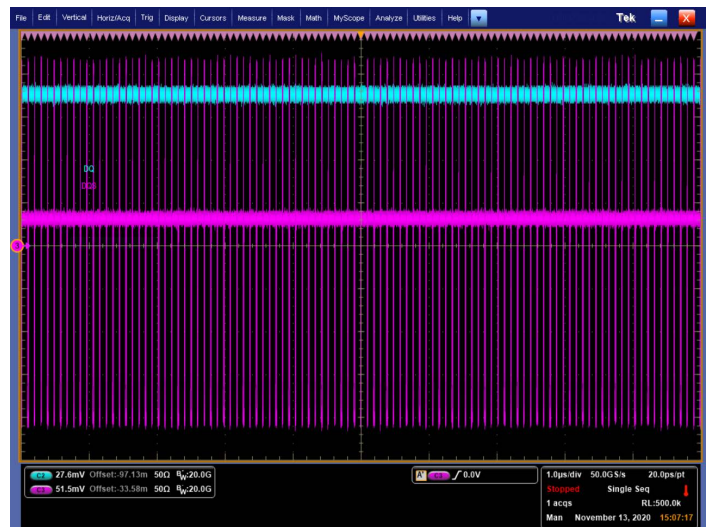
Burst detection



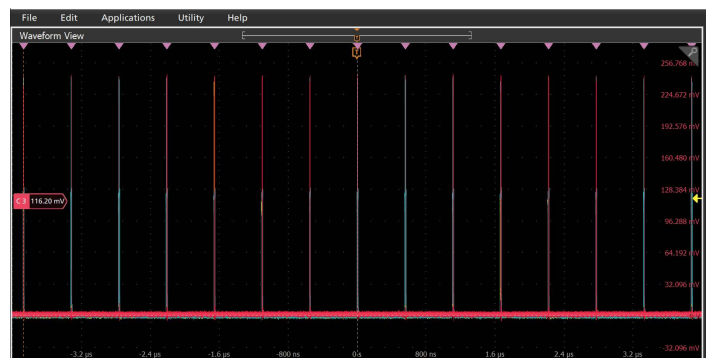
Automated Write Burst detection on MSO/DPO70000 Series



Write Burst detection on 7 Series scope, model DPO714AX



Automated Read Burst detection on MSO/DPO70000 Series



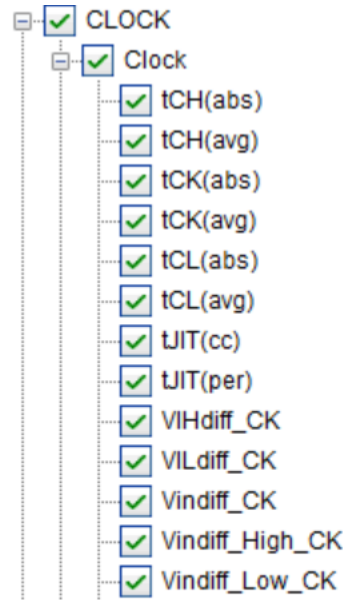
Read Burst detection on 7 Series scope, model DPO714AX



Visual trigger

Test selection

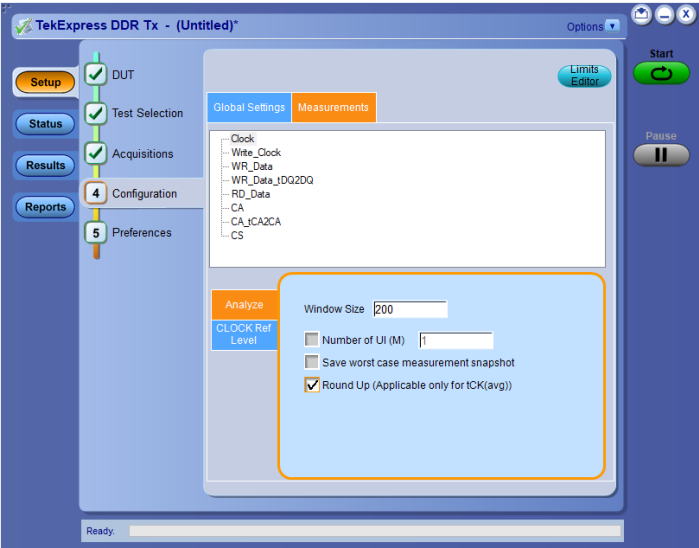
The TekExpress DDR Tx test selection panel allows the user to select the various measurements supported by the application.



Test selection panel – tree view of measurements

Configurations

Ease of use measurement configuration to configure measurements by group instead of running through all the 50+ measurements.



Results and reporting with waveform

The measurement configurations and JEDEC pass/fail limits are automatically applied for the selected measurements based on the memory specification and the selected speed grade. The results report includes DDR measurements of statistical data, measurement plots, and the screenshot of the waveforms with the cursors. Hyperlinks within the report allow you to navigate between the sections.

When test execution is complete, the application automatically opens the Results panel and displays the summary of test results.

Test Name	Measureme...	Pass/Fail	Iteration	Value	Margin
tCH(abs)	tCH(abs) Min,Ch3	Pass	1	497.72 mtCK (avg)	0.06772 tCK (avg)
tCH(avg)	tCH(avg) Min,Ch3	Pass	1	499.75 mtCK (avg)	0.03975 tCK (avg)
tCK(abs)	tCK(abs) Min,Ch3	Pass	1	1.2473 ns	0.0673 ns
tCK(avg)	tCK(avg) Mean,Ch3	Pass	1	1.25 ns	0.019875 us
tCL(abs)	tCL(abs) Max,Ch3	Pass	1	502.09 mtCK (avg)	0.06791 tCK (avg)
tCL(avg)	tCL(avg) Max,Ch3	Pass	1	500.24 mtCK (avg)	0.03976 tCK (avg)

Measurement results

Tektronix® TekExpress DDR Tx Transmitter Test Report			
Test Information			
Test ID	Clock Differential Correlation	Scope Model	DPO7000
Test Time	8/22/2023 2:02:12 AM	Scope Serial Number	00400109
Hardware Type	LPDDR5-5X	Test Fixture Configuration	PA03
Test Express Version	TestExpress 5.11.0.14	Scope Firmware Version	CX00_1CT_FV-2_00-2_release_2735
App Version	DDR Tx 1.2.0.1	Check Signal Pathing	Differential
JEDEC Spec Version	DPO7000-1E	WCK/CK00 Signal Pathing	Differential
Test Signal	U0A	Data Rate	1200 MT/s
User Defined Acquisition	Disabled	Clock Frequency	400 MHz
Overall Execution Time	00:00:04	WCK Frequency	1200 MHz
Overall Test Result	Pass	WCK Check	A-1
Test Comment: General Comment - DDR Tx			
Probe Information			
Probe	Signal	Probe Type	Probe Serial Number
CP01	CK00	"TECA2220"	"N/A"
CP02	-	"TECA2220"	"N/A"
CP03	-	"TECA2220"	"N/A"
CP04	-	"TECA2220"	"N/A"
Test Matrix Summary Table			
jeu0a00	Pass		
jeu0a01	Pass		
jeu0a02	Pass		
jeu0a03	Pass		
jeu0a04	Pass		
jeu0a05	Pass		
jeu0a06	Pass		
jeu0a07	Pass		
jeu0a08	Pass		
jeu0a09	Pass		
jeu0a10	Pass		
jeu0a11	Pass		
jeu0a12	Pass		
jeu0a13	Pass		
jeu0a14	Pass		
jeu0a15	Pass		
jeu0a16	Pass		
jeu0a17	Pass		
jeu0a18	Pass		
jeu0a19	Pass		
jeu0a20	Pass		

Measurement report

Verification versus debug

The TekExpress DDR Tx application provides a comprehensive set of JEDEC timing and electrical measurements for the LPDDR5-5X standard. It provides access to the DPOJET Advanced Jitter and Timing analysis engine that allows flexibility to reconfigure the existing measurements or to perform new measurements that are not defined by the JEDEC specification using new user-specified test limits.

Oscilloscope triggering and waveform identification

The Tektronix Pinpoint® trigger system provides the most comprehensive high-performance trigger system in the industry. The Pinpoint trigger system encompasses threshold and timing related triggers, Dual A and B Event Triggering, Logic Qualification, Window Triggering, and Reset Triggering.

The Advanced Search and Mark feature in the Tektronix MSO/DPO5000, DPO7000, MSO/DPO70000 series, and 7 Series DPO oscilloscopes find unique events in the waveforms. It scans acquired waveform data for multiple occurrences of an event and marks each occurrence.

The Search and Mark feature has a close relationship with the Pinpoint trigger system since they both can be used to discriminate signal characteristics. Search and Mark includes signal-shape discrimination features of the Pinpoint trigger system and extends them across live channels, stored data, and math waveforms.

The Visual Trigger makes the identification of the desired waveform events quick and easy by scanning all the acquired analog waveforms and comparing them with the geometric shapes on the display. By discarding the acquired waveforms which do not meet the graphical definition, Visual Triggering extends the oscilloscope's trigger capabilities beyond the traditional hardware trigger system. This feature is currently supported only on MSO/DPO70000 SX/DX oscilloscope models.

Specifications

Supported oscilloscopes

- 7 Series scope, model DPO714AX at 16 GHz, 20 GHz, and 25 GHz
- MSO71604DX, MSO72004DX, MSO72304DX, MSO72504DX, and MSO73304DX
- DPO73304DX
- Non-ATI channels of DPO75002SX, DPO75902SX, DPO7702SX, DPS75004SX, DPS75904SX, DPS77004SX and DPO73304SX

Data rate	Minimum bandwidth	Channels	Description
Up to 8533 MT/s	16 GHz	4	• 7 Series scope, model DPO714AX • MSO71604DX

Recommended probes

Active probes	Description
P7720	20 GHz TriMode probe with TekFlex connector technology
P7716	16 GHz TriMode probe with TekFlex connector technology

Probe tips	Description
P77STFLXA/P77STCABL	Active, Solder-in Tip with TekFlex connector technology, probe tips to probe directly on the motherboard/vias or interposers with 0 Ω resistor.
P77STFLXB/P77STLRCB	Active, Solder-in Tip with TekFlex connector technology, probe tips to probe on the SI Interposer with 100 Ω resistor (Nexus XH Series Interposer).
P77STFLRA	Active, long reach solder-in tip with TekFlex connector technology
P77HTFLRA	Active, long reach high temperature solder-in tip with TekFlex connector technology
P77STFLRB	Active, long reach 55 Ω Solder-in tip with TekFlex Connector technology for DDR/LPDDR electrical Validation with interposers
P77HTFLRB	Active, long reach 55 Ω Solder in tip with TekFlex Connector technology for high-temperature DDR/LPDDR electrical Validation with interposers (up to 125 °C)
SI Interposer	EdgeProbe™, Direct Attach, and Socketed Interposer are available from Nexus. Order directly from Nexus. Request the s-par files for all individual signals on the interposer instead of getting a generic nominal s-par model. Refer the Nexus's page for more information: www.nexustechology.com/products/memory-interposers/lpddr5-mobile-memory-interposers/

Ordering information

To order on 7 Series scope, model DP0714AX

Nomenclature	Description
7 Series DPO >= 16 GHz	
7-CMLPDDR5SYS	License; LPDDR5 and 5x System Transmitter Test (Tx) Automated Compliance Solution using TekExpress Framework; Canned, Electronically Downloaded; Requires options 7-DJA, 7-SIMA and 7-WIN; Node Locked
7-CMLPDDR5SYS-FL	License; LPDDR5 and 5x System Transmitter Test (Tx) Automated Compliance Solution using TekExpress Framework; Canned, Electronically Downloaded; Requires options 7-DJA, 7-SIMA and 7-WIN; Floating

To order on DPO/MS070000 Series

Nomenclature	Description
SX, DX >= 16 GHz	
DPO-UP LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO73304SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO73304DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO75002SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO75902SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPO7702SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
MSO72304DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
MSO71604DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
MSO72004DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
MSO72504DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
MSO73304DX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPS75004SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPS75904SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)
DPS77004SX LPDDR5SYS	License: LPDDR5 TekExpress Compliance/Debug Automation Memory Bus Electrical Validation and Analysis Software (require options SDLA64, DJA, and VET)

To order floating licenses on existing DPO/MS070000 Series

Product Nomenclature	Description	Mapped Options	Required Options
DPOFL-LPDDR5SYS	License; LPDDR5 System-level Tx TekExpress Compliance/Debug Automation Software; Floating	LPDDR5SYS	SDLA64, DJA, and VET

Table continued...

Product Nomenclature	Description	Mapped Options	Required Options
DPOFT-LPDDR5SYS	License; LPDDR5 System-level Tx TekExpress Compliance/ Debug Automation Software; Floating Trial	LPDDR5SYS	SDLA64, DJA, and VET

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Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.

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CalPlus GmbH
Zentrale Berlin
Heerstraße 32 • 14052 Berlin
Tel.: 030 214982-0 • Fax: 030 214982-50
office@calplus.de • www.calplus.de

CalPlus GmbH
Niederlassung ScopeShop
Normannenweg 30 • 20537 Hamburg
Tel.: 040 3039595-0 • Fax: 040 3039595-50
scopeshop@calplus.de • www.calplus.de

* European toll-free number. If not accessible, call: +41 52 675 3777

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