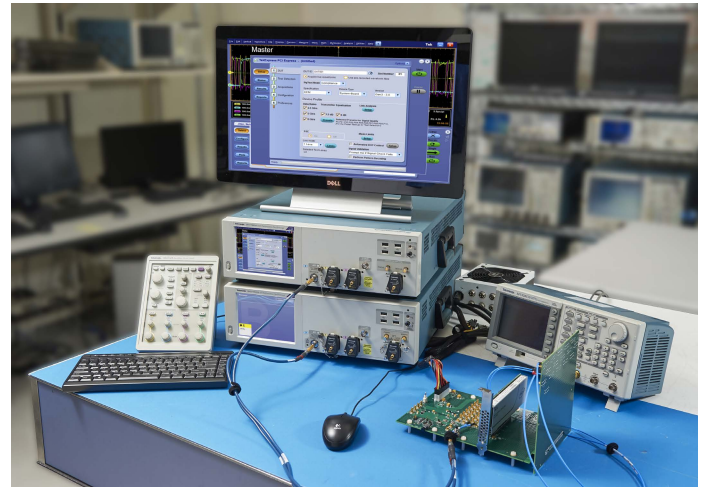
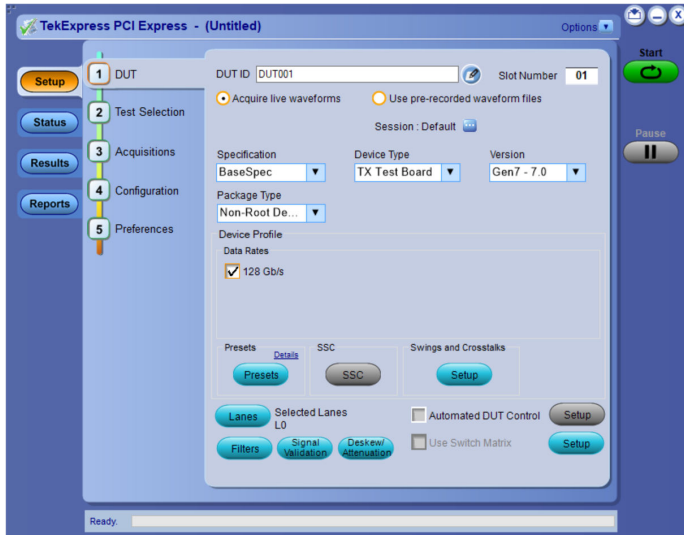


# TekExpress PCI Express® Tx Compliance/Debug Test Solution

## 7 Series DPO and DPO-MSO70000 Datasheet



PCI Express (PCIe) 7.0 continues to use four-level pulse amplitude modulation (PAM4) signaling to achieve a data rate of 128 GT/s, while maintaining backward compatibility with non-return-to-zero (NRZ) signaling used in earlier generations (PCIe 1.0 - 5.0) and with PAM4-based implementations in PCIe 6.0. PAM4 signaling introduces new signal integrity challenges for both design and validation. Tektronix PCIe 7.0 compliance testing software reduces these challenges through automated testing that ensures measurement accuracy and repeatability.

The software options PCE7 (Gen 7.0), PCE6 (Gen 6.0), PCE5 (Gen 5.0), PCE4 (Gen 4.0), and PCE3 (Gen 1.0/2.0/3.0) on the MSO/DPO70000 Series oscilloscope applications provide the most comprehensive solution for PCIe transmitter and system Reference Clock compliance testing, as well as for debug and validation of PCIe devices per the PCI-SIG® Base & CEM specifications.

Option 7-CMPCIE1234 on the 7 Series DPO enables PCIe Gen 1.0 to Gen 4.0 transmitter and System Reference Clock compliance testing per the PCI-SIG® Base and CEM specifications.



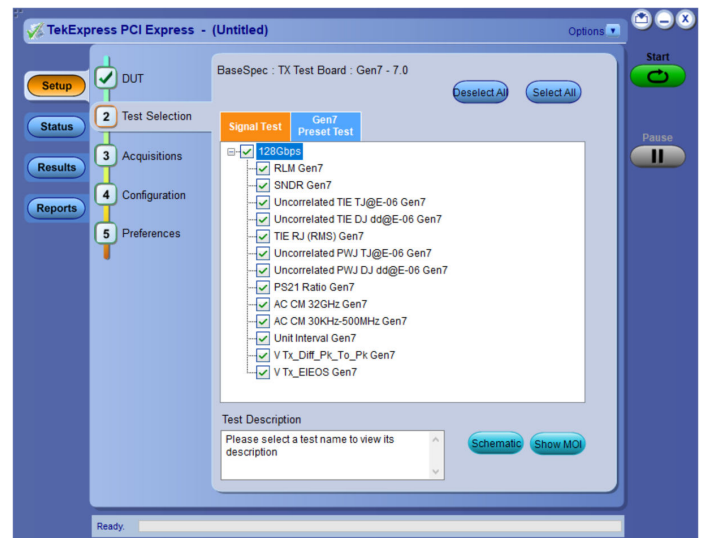
### Features and benefits

- Support for PCIe Gen 7.0 Base transmitter testing for the Tektronix DPO70000 Series oscilloscopes
- Support for PCIe Gen 1.0 to Gen 6.0 Base and CEM transmitter testing for the Tektronix MSO/DPO70000 Series oscilloscopes as per the bandwidth requirements
- System Reference Clock Jitter and signal integrity measurements for Gen 1.0 to Gen 6.0 using:
  - Intel Clock Jitter Tool
  - Skyworks PCIe Clock Jitter Tool
  - Tektronix DPOJET (Supported only for MSO/DPO70000 models)
- 128 GT/s and 64 GT/s (PAM4) signal integrity measurements using PAMJET/DPOJET on MSO/DPO70000 oscilloscopes
- Gen 6.0 Tx Equalization Preset test uses the Linear Fit Pulse Response (LFPR) method on MSO/DPO70000 oscilloscopes

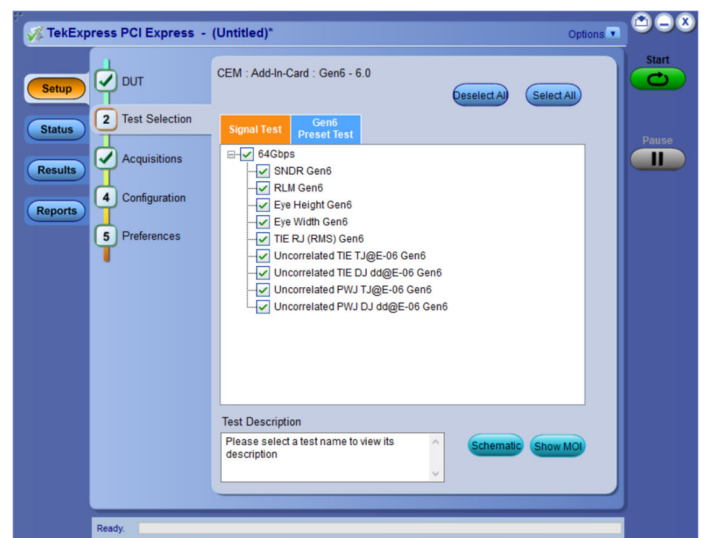
- Autoset oscilloscope for both vertical and horizontal scales for accurate and specification compliant measurements
- Automated acquisition and waveform management to simplify testing across supported data rates, Tx compliance patterns, and lane widths
- Automated DUT control to step through data rates and compliance patterns
- RF switch automation of PCIe Gen 3.0 to Gen 5.0 test solution, supports up to x16 lanes on MSO/DPO70000 Series oscilloscopes. PCI Gen 3.0 and Gen 4.0 RF switch automation is supported on 7 Series DPO oscilloscopes
- Support for NVMe and CXL physical layer testing
- De-embed the impact of a break-out channel, test fixtures, and cables to achieve measurements at the test point of interest (requires Option SDLA Serial Data Link Analysis)
- Flexible test selection: configurable list of test items per the Base specification and CEM specification. This enables retesting of measurements of interest
- SigTest integration: Uses SigTest EXE (using command line interface) to perform the analysis of acquired waveforms, providing the ability to test a system using the PCI-SIG®-recommended analysis tool
- Enable parallel waveform analysis for faster test throughput
- Support both AC fit & DC method for measuring PCIe 5.0 Tx Preset on MSO/DPO70000 oscilloscopes
- Generates a single test report with a pass/fail summary, along with detailed informative test items and eye diagrams
- A summary table at the top of the report provides a quick overview of the results for normative measurement
- Pattern matching: Verifies that the transmitter sends the correct set of compliance patterns before acquiring signals for compliance analysis. This feature supports PCIe Gen 3.0 only
- PHY level protocol decode: Decodes and displays the PCIe data in a protocol-aware view. A time-correlated event table view with waveforms allows for quickly searching through events of interest. This feature supports up to Gen 3.0 only on MSO/DPO70000 oscilloscopes
- Multi-lane testing: Perform analysis on multiple lanes of PCIe data to speed up the Tx analysis in a multi-lane system
- Compliance and debug: Provides a toolkit of DPOJET-based setups to quickly switch into debug and validation mode when a DUT fails compliance on MSO/DPO70000 oscilloscopes
- Comprehensive programmatic interface: Enables automation of programs and scripts to call PCIe related TekExpress functions

## Applications

Tektronix provides the most comprehensive solutions for PCIe transmitter validation and compliance of at the Base (silicon) and system level including support for CEM, U.2, and M.2 interfaces. Numerous protocols use the PCIe physical layer, including NVMe and CXL, and can take advantage of the transmitter and Reference Clock automation under TekExpress software solution.



**TekExpress PCIe test selection for compliance test analysis**



**Gen 6.0 CEM measurements of signal test**



### Gen 6.0 CEM measurements of preset test

The Tektronix Option 7-CMPCIE1234 on 7 Series DPO and PCE3 (Gen 1.0/2.0/3.0), PCE4, PCE5, PCE6 and PCE7 on MSO/ DPO70000 Series oscilloscopes includes compliance and debug testing and electrical validation for the following:

- Root complex base Tx jitter and voltage
- Endpoint base Tx jitter and voltage
- Switches
- Bridges
- Add-In cards
- System boards
- Embedded systems
- Express module

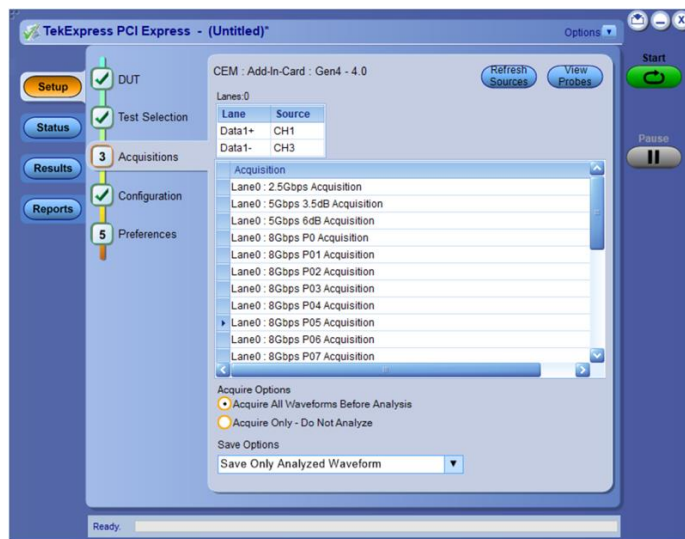
The Tektronix applications include a TekExpress™ compliance automation solution that integrates SigTest from the PCI-SIG as well as Tektronix DPOJET-based PCIe Jitter and eye diagram analysis tools for debug purposes in a single software package.

On MSO/DPO70000 Series oscilloscopes, TekExpress™ compliance automation is available for the following PCIe generations:

- Gen 1.0 – Gen 3.0 CEM and Gen 3.0 Base via Option PCE3
- Gen 4.0 Base and CEM via Option PCE4
- Gen 5.0 Base and CEM via Option PCE5
- Gen 6.0 Base and CEM via Option PCE6
- Gen 7.0 Base via Option PCE7

On 7 Series DPO oscilloscopes, TekExpress compliance automation is available for PCIe Gen 1.0 - 4.0 Base and CEM via Option 7-CMPCIE1234.

These options are designed to meet the challenges of the next generation of serial data standards such as PCIe. The Tektronix MSO/DPO70000 Series of oscilloscopes is approved by PCI-SIG for compliance testing. These oscilloscopes provide the industry's leading vertical noise performance with the highest number of effective bits (ENOB) and flattest frequency response for oscilloscopes in their class.



### TekExpress oscilloscope acquisition setup

## Compliance testing

The PCI-SIG provides PCIe compliance tests for testing PCIe CEM form factor, including system and add-in-card (AIC). To be listed on the Integrators List, the PCIe system or device must pass interoperability and compliance testing. For electrical validation, the PCI-SIG uses SigTest Post Capture Analysis Software that uses acquisitions from an oscilloscope connected to the PCI-SIG's CBB (main board + riser) test fixture for add-in cards or CLB test fixture for systems to perform the analysis. Manually capturing the required waveforms and analyzing them is tedious, time consuming, and error prone.

Tektronix TekExpress Automation software for PCIe transmitter Compliance reduces the effort and accelerates the compliance testing for PCIe systems and devices with several unique and innovative capabilities. These options ultimately allow the testing of devices that support various technologies, such as NVMe, which is supported as an add-in card device, or through a U.2 or M.2 connector.

The Tektronix TekExpress Automation software can control the DUT using selected models of a Tektronix AFG (Arbitrary Function Generator) or AWG, GRL PCIE 3/4 controller Anritsu Z2025A CBB controller, or NI USB6501 CBB controller, or integrated AFG in DPO7 series scope (only for DPO7 series scope) to toggle DUT and automatically cycle it through various speeds, de-emphasis, and presets that are necessary for the compliance test. This

eliminates the error-prone manual approach used for DUT control on the CBB and CLB test fixtures. This feature supports both CEM and Base testing.

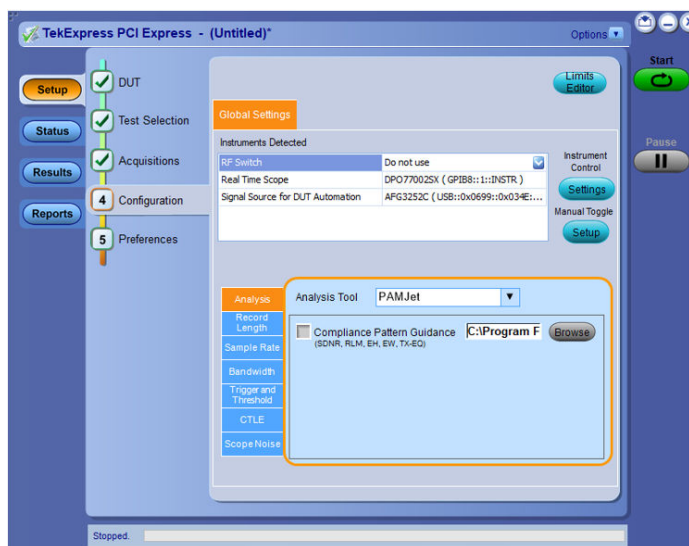
A complete test run requires multiple waveforms to be acquired at different DUT settings per lane. This waveform set will increase by the number of lanes that need to be analyzed. The ability to manage and store the required data for analysis and future reference is an important criterion for any compliance solution. The TekExpress automation software, apart from adjusting the horizontal and vertical settings as well as the acquisition depth for optimal signal quality for accurate analysis, provides easy analysis to manage multiple acquired waveforms.

The Tektronix TekExpress automation software uses the PCI-SIG's SigTest EXE to analyze the acquired waveforms. This makes the analysis result consistent with the SigTest post-capture analysis software used at PCI-SIG workshops for compliance testing.

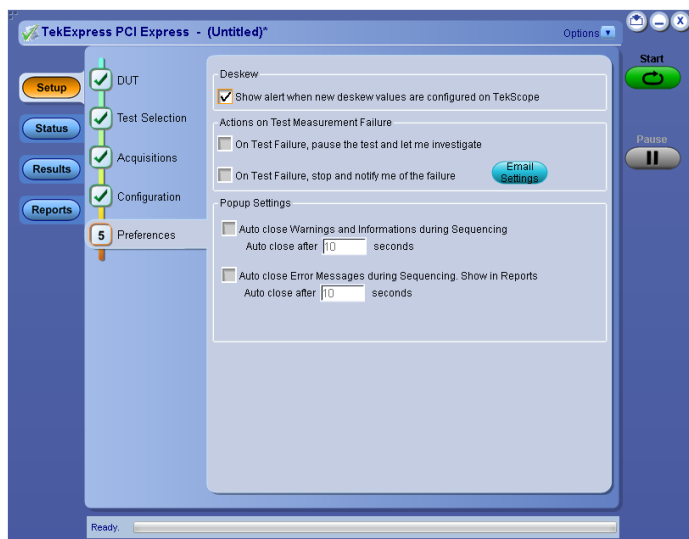
TekExpress automation software provides flexibility in selecting data rates, voltage swing, presets, and the tests to run. It also provides the option to de-embed the effects of the channel and the test fixtures and provide an accurate representation of the signal at the pins as required by the specification.

PCE7 and PCE6 TekExpress uses Tektronix PAM analysis tool PAMJET for the measurement. During analysis, TekExpress will automatically set up the tool as per the specification, capture results, and report them to the user. PAMJET also allows expert users to configure the PAMJET tool to test the DUT in custom settings for debugging purposes.

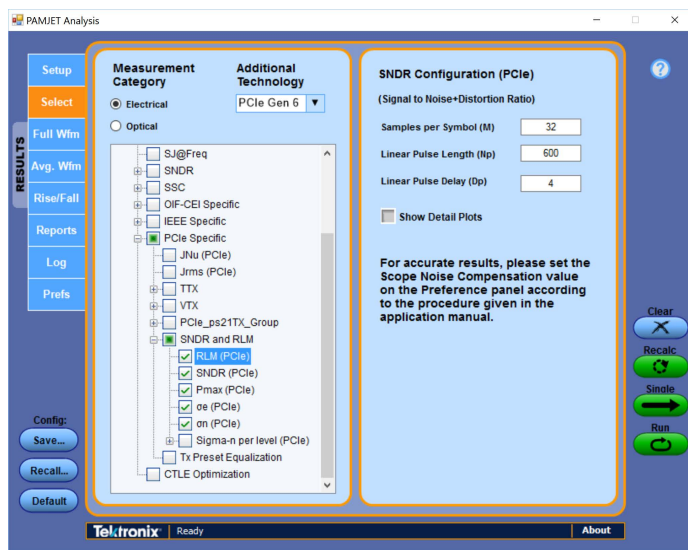
PAMJET introduces the Signal to Noise Distortion Ratio (SNDR) measurements with measurement methodology updated to support the PCIe Gen 7.0 Base and PCIe Gen 6.0 Base and CEM specifications. Support for instrument noise compensation is integrated to improve measurement accuracy.



**TekExpress setup configuration**

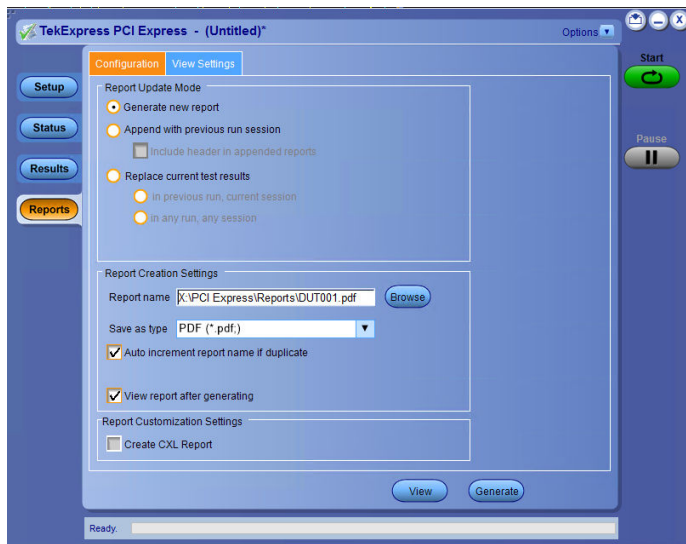


**TekExpress setup preferences**



**Selection of measurement category in PAM4 transmitter analysis**

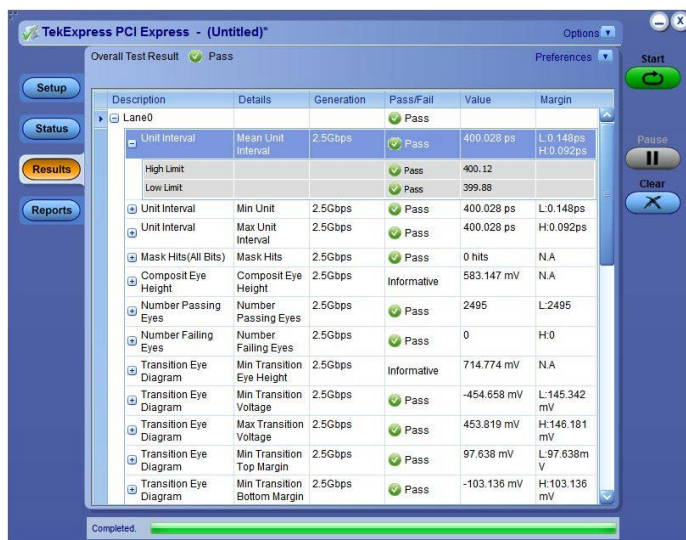
All the analysis results are compiled in a PDF/HTML/CSV formatted report that can include pass/fail summary, eye diagrams, setup configuration, and user comments. The contents of the report can be customized to include information of interest such as append results and custom report generation based on test name pass/fail equalization.



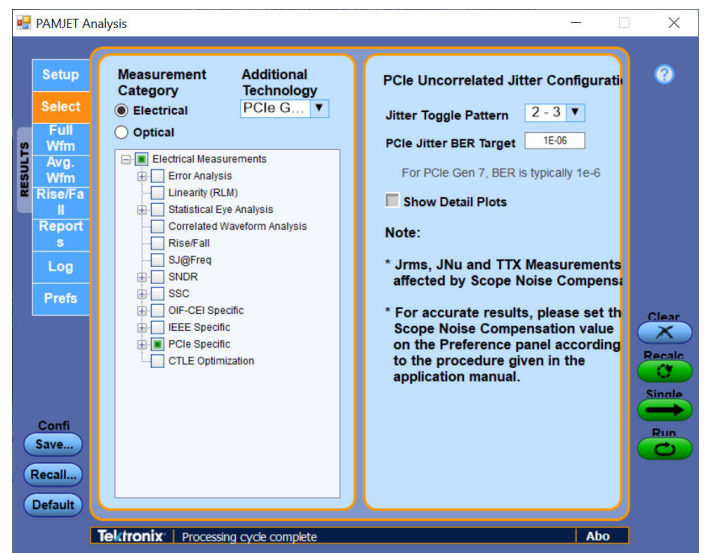
**TekExpress report generation preferences**



**PAMJET PCIE analysis**



**TekExpress results summary**



**PAMJET measurements**

## PAMJET for PCIe measurements

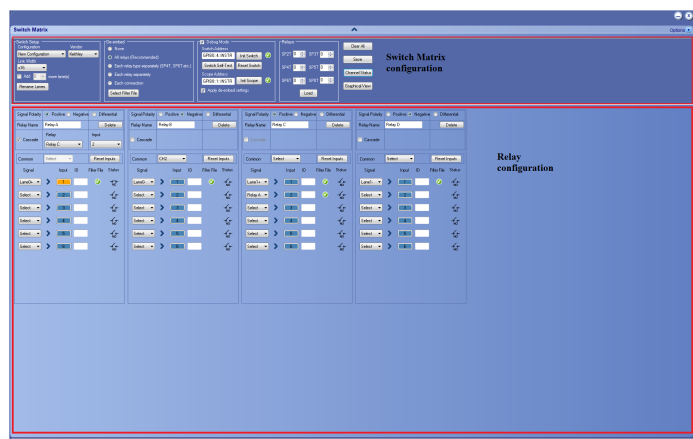
Tektronix PAMJET is an industry-leading PAM analysis tool with best in class clock recovery and integrated configurable reference receiver, which is used for Gen 6.0 and Gen 7.0 measurements. This PAMJET tool can configure the measurements, perform Bessel Thompson filtering, clock recovery, CTLE, pattern guidance, and report the results. These built-in functions are specifically designed to aid the Gen 7.0 Base and Gen 6.0 Base and CEM testing.

## System Reference Clock Testing with TekExpress

Reference Clock testing is moved from optional to required for many designs due to the jitter limit decrease driven by the highest data rates supported by the PCI-SIG standards. Additionally, with the removal of dual-port (data and clock Tx testing) for Gen 5.0 systems, compliance is required on the Reference Clock. The TekExpress PCIe solution has now integrated the Intel CJT and Skyworks Clock Jitter Tool to allow an automated hassle-free Reference Clock testing. Once the user connects the Reference Clock output to the oscilloscope, the TekExpress PCIe software will acquire the signal, invoke the Intel CJT or Skyworks Clock Jitter Tool, and provide Reference Clock test results from Gen 1.0 to Gen 6.0. Instrument noise compensation is supported with both the tools.

Switch Matrix automation

The Switch Matrix application configures and sets up automated multi-lane testing using an RF switch. The solution allows you to map each of the several transmitter signals and forward the selected input either to another relay or to the oscilloscope channel. Options SWX-PCE and 7-SWX-PCIE support x12 and x16 lanes. Minicircuits supports up to Gen 5.0 switches and enhances throughput and automated test speed.



Switch Matrix application settings



Switch configuration example

Debug and validation

If a DUT fails any portion of the compliance test, the application includes a DPOJET-based debug and analysis toolkit customized for debug and validation of PCIe interfaces on MSO/DPO70000 oscilloscopes.

The Jitter measurements introduced with PCIe Gen 3.0 and Gen 4.0 provide separate limits for data dependent (DDJ) and uncorrelated deterministic jitter (UDJDD). It is important to separate DDJ (which can be compensated with transmitter and receiver equalization) and UDJDD (which can be caused by effects such as crosstalk and power supply noise).

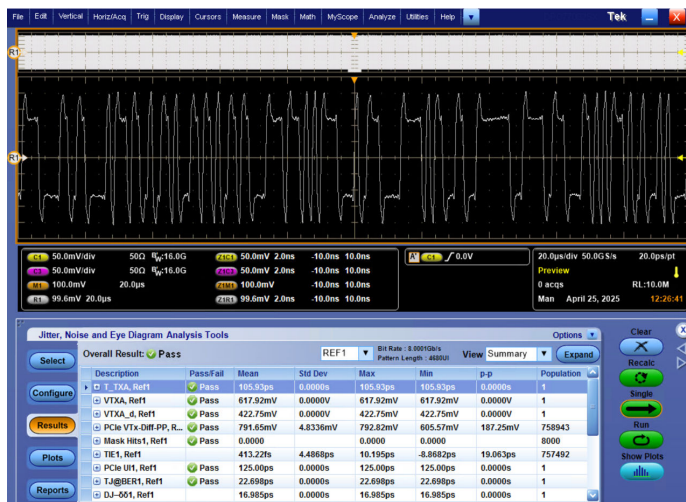
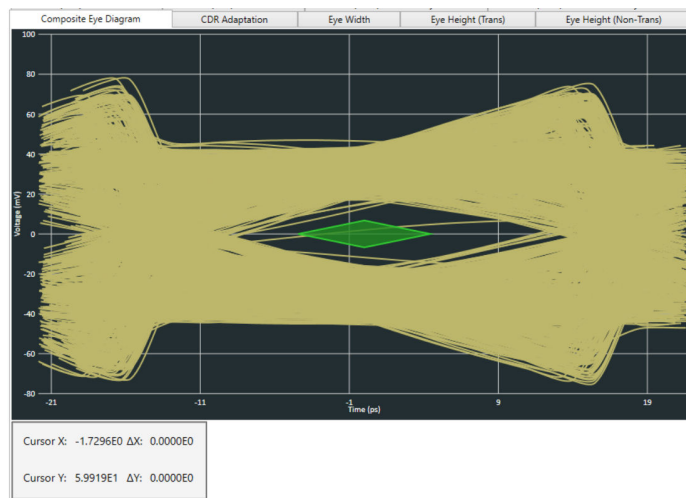
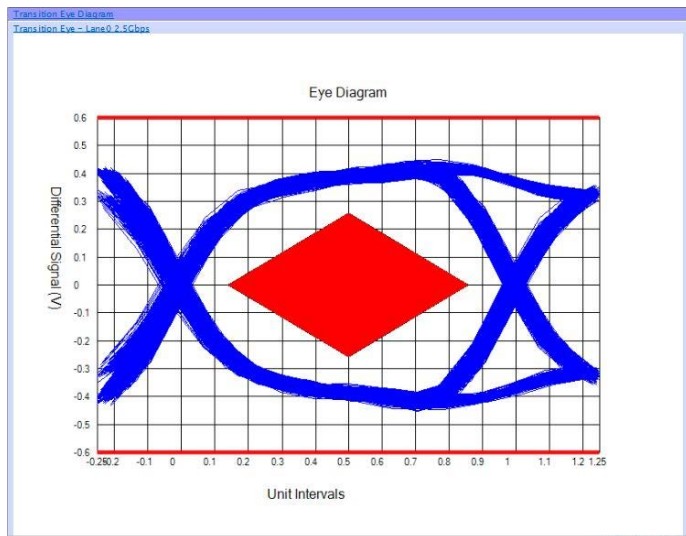
Apart from the above Jitter measurements, Pulse Width Jitter (PWJ) is a new measurement that addresses the increased channel loss at 8 to 16 Gb/s. The purpose of the PWJ measurement is to ensure that lone bits meet minimum pulse width requirements. All new jitter measurements implement Q-scale extrapolation as defined in the base specification. The Tektronix Option PCE3, Option PCE4, Option PCE5, Option PCE6, and Option PCE7 provide the complete set of PCIe 3.0, 4.0, 5.0, 6.0, and 7.0 Base Spec Jitter measurements enabling silicon designers to verify that their silicon meets the base specification requirements.

Furthermore, the base specification requirements are defined at the pins of the transmitter. Before the measurements are computed the test channel must be de-embedded. De-embed filters can be easily created using the Tektronix Option SDLA64 Serial Data Link Analysis software and then quickly entered into the Option PCE3, and Option PCE4 base specification measurement setup and saved for future use. In addition to Jitter, Option PCE3, and Option PCE4 also provide voltage, package loss, and transmitter equalization measurements.

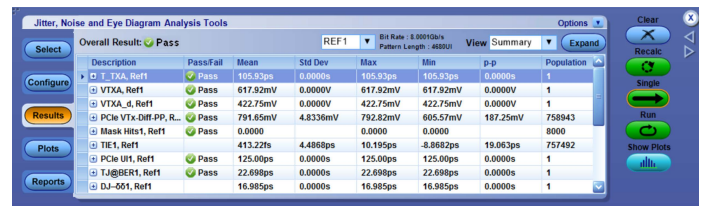
Option PCE3 and Option PCE4 leverage the channel modeling and receiver equalization functionality of the Tektronix Option SDLA64 software to support CEM measurements. Unlike other solutions, Option PCE3, Option PCE4 and Option CMPCIE1234 provide full visibility to the signal as it is modified to embed the compliance channel and provide receiver equalization. Eye diagrams and measurements can be set up to visually see the results of channel embedding, CTLE application, and DFE. For example, when determining the optimal Rx Equalization settings (CTLE setting and DFE tap value) the resulting eye diagrams and measurements show the effects of post processing on the acquired signal. Compliance measurements can then be taken on the waveform.

| TekExpress PCIe Tx<br>TX Test Board Test Report |                         |                         |                  |
|-------------------------------------------------|-------------------------|-------------------------|------------------|
| Setup Information                               |                         |                         |                  |
| DUT ID                                          | DUT001                  | Fixture Type            | Non Gen5         |
| Date/Time                                       | 9/1/2025 2:09:15 AM     | Scope Model             | DPO7002SX        |
| Device Type                                     | BaseSpec                | Scope Serial Number     | B321905          |
| TekExpress PCIe Tx Version                      | v12.0.0.4               | SPC Factory Calibration | PASS PASS        |
| TekExpress Framework Version                    | v5.12.0.22              | Scope FW Version        | v10.15.0 Build 3 |
| TekExpress Execution Mode                       | Live                    | DPOJET Version          | v10.5.0.2        |
| Compliance Mode                                 | No                      | Channel Info            | ATI              |
| Spec Version                                    | Gen5 - 6.0              | Probe CH1 Model         | none             |
| Voltage Swing                                   | Reduced                 | Probe CH1 Serial Number | N/A              |
| SSC Status                                      | Off                     | Probe CH2 Model         | none             |
| SlotNumber                                      | 01                      | Probe CH2 Serial Number | N/A              |
| Acquisition Count                               | 1                       | Toggle Mode             | Manual           |
| Deembed Automation                              | Disabled                | PAMJET Version          | v10.10.1.826     |
| Deembed Value                                   | CH1 : 0 ps, CH2 : 21 ps |                         |                  |
| Embed Filter File                               | N/A                     |                         |                  |
| DeEmbed Filter File                             | N/A                     |                         |                  |
| Jitter - CTLE Optimization Mode                 | Auto                    |                         |                  |
| PWJ - CTLE Optimization Mode                    | Auto                    |                         |                  |
| Overall Test Result                             | Fail                    |                         |                  |
| Overall Execution Time                          | 01:02:29                |                         |                  |
| DUT COMMENT                                     |                         | DUT001                  |                  |

TekExpress PCI Express test report



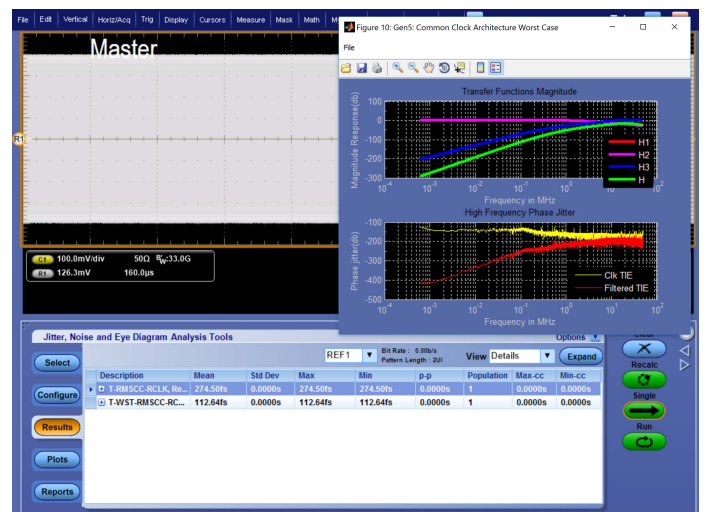
DPOJET PCE3 base specification measurement suite



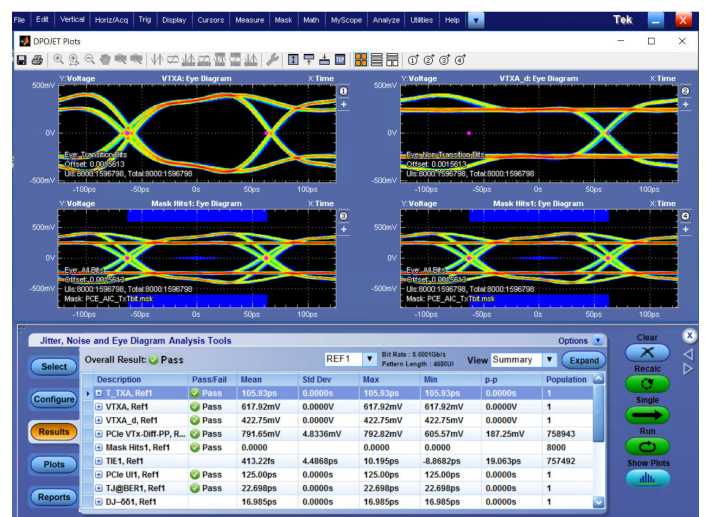
DPOJET PCE3 base specification measurement suite

## DPOJET based Reference Clock measurements

On MSO/DPO70000 oscilloscopes, Tektronix DPOJET based Reference Clock measurements provide a reliable way to implement the Reference clock specifications described in the PCIe Base Specification Rev 1.0 for Gen 1.0, Gen 2.0, Gen 3.0, Gen 4.0 and Gen 5.0.



Example of RefClk measurements, together with generated plots



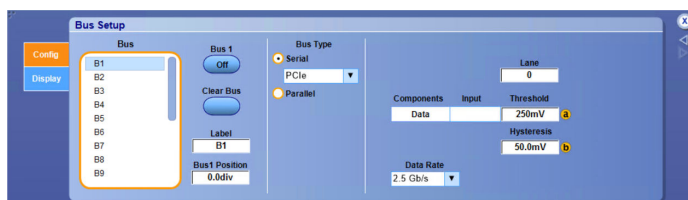
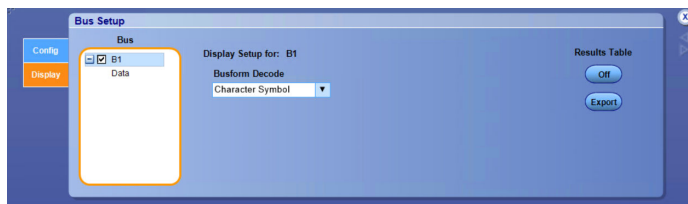
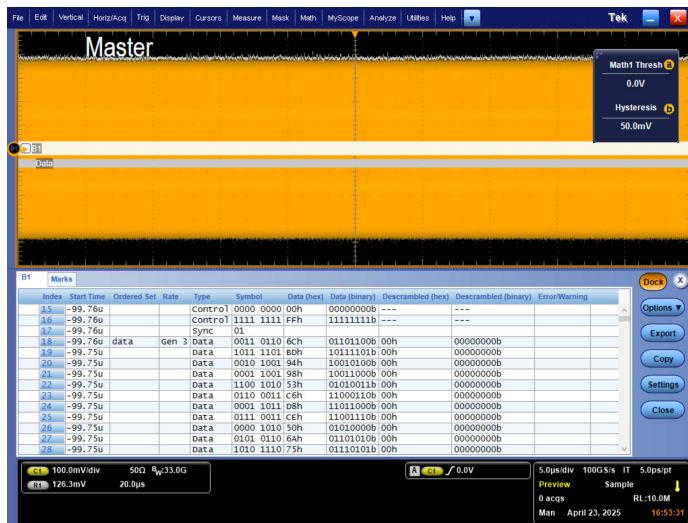
DPOJET measurements and their plots

## Comprehensive programmatic interface

You can use Standard Commands for Programmable Instruments (SCPI) to communicate with the TekExpress application. The Online Help document of TekExpress application describes the steps for TCP/IP socket configuration and TekVISA configuration to execute the SCPI commands.

## PCIe Decoder for Gen 1.0 - 4.0 (Option SR-PCIe)

On MSO/DPO70000 Series oscilloscopes, Decode and Display of PCIe data in a protocol-aware view with the characters and names familiar from the standard including ordered sets such as SKP, Electrical Idle, and EIEOS. A time-correlated event table view with waveform allows for quickly searching through events of interest simultaneously. All decoding features support PCIe generations 1.0 - 4.0. The PCIe trigger is easily configured through Bus Setup under the oscilloscope's Vertical menu with a variety of user-adjustable settings. The PCIe data stream is integrated with serial bus trigger and search for PCIe Gen 1.0 and Gen 2.0 allows for triggering on information of interest. This option is available only on MSO/DPO70000DX and SX oscilloscopes



## Comprehensive measurements for PCIe validation, debug, and precompliance

Tektronix Option PCE3, Option PCE4, Option PCE5, Option PCE6, and Option PCE7 provide measurements that span multiple test points and versions of the PCIe specification. All PCIe specifications, test points, and measurements supported are listed in the following sections.

| Test method | Spec revision       | PCIe specification title                                 | Test points defined                                      |
|-------------|---------------------|----------------------------------------------------------|----------------------------------------------------------|
| Rev 1.1     | Rev 1.1             | Base Specification                                       | Transmitter and Receiver                                 |
|             | Rev 1.1             | CEM Specification                                        | System and Add-in Card Reference Clock                   |
|             | Rev 1.0             | Express Module Specification                             | Transmitter Path and System Board                        |
|             | Rev 1.0             | PCMCIA Express Card Standard                             | Host System Transmitter<br>Express Card Transmitter      |
|             | Ver. 3.0<br>Rev 1.1 | Mobile PCIe Module (MXM) Electromechanical Specification | PCIe                                                     |
| Rev 2.0     | Rev 1.0             | External Cabling Specification                           | Transmitter and Receiver Path                            |
|             | Rev 2.0             | Base Specification                                       | Transmitter and Receiver<br>Mobile Low-power Transmitter |
|             | Rev 2.0             | CEM Specification                                        | System and Add-in Card (3.5 and 6 dB de-emphasis)        |
|             | Ver. 3.0<br>Rev 1.1 | Mobile PCIe Module (MXM) Electromechanical Specification | PCIe                                                     |
|             | Rev 3.0             | Test Specification                                       | System and Add-in Card                                   |
| Rev 3.0     | Rev 1.0             | Base Specification                                       | Transmitter                                              |
|             | Rev 1.0             | CEM Specification                                        | System and Add-in Card                                   |
|             | Rev 3.0             | Test Specification                                       | System and Add-in Card                                   |
| Rev 4.0     | Rev 1.0             | CEM Specification                                        | System and Add-in Card                                   |

| Test method | Spec revision | PCIe specification title | Test points defined |
|-------------|---------------|--------------------------|---------------------|
| Rev 5.0     | Rev 1.0       | Base Specification       | Transmitter         |
|             | Rev 1.0       | CEM Specification        | Transmitter         |
| Rev 6.4     | Rev 1.0       | Base Specification       | Transmitter         |
|             | Rev 1.0 - CEM | CEM Specification        | Transmitter         |
| Rev 7.0     | Rev 1.0       | Base Specification       | Transmitter         |

## Specifications

All specifications apply to all models unless noted otherwise.

### Supported Reference Clock measurements

| Generation | Architecture         | Measurements             | Limits    |
|------------|----------------------|--------------------------|-----------|
| PCIe 1.1   | Common clock         | T-CC- RCLK               | Specified |
|            |                      | T-WST-CC- RCLK           | Specified |
|            | Independent RefClock | IR2.5GBPS                | Specified |
| PCIe 2.1   | Common clock         | T-RMSSC-RCLK-5GBPS       | Specified |
|            |                      | T-WST-RMSSC-RCLK-5GBPS   | Specified |
|            | Independent RefClock | IR5GBPS                  | Specified |
| PCIe 3.1   | Common clock         | T-RMSSC-RCLK             | Specified |
|            |                      | T-WST-RMSSC-RCLK         | Specified |
|            | Independent RefClock | IR8GBPS                  | Specified |
| PCIe 4.0   | Common clock         | PCIE4_T-RMSSC-REFCLK     | Specified |
|            |                      | PCIE4_T-WST-RMSSC-REFCLK | Specified |
|            | Independent RefClock | IR16GBPS                 | Specified |
| PCIe 5.0   | Common clock         | PCIE5_T_RMSSC-REFCLK     | Specified |
|            |                      | PCIE5_T-WST-RMSSC-REFCLK | Specified |
|            | Independent RefClock | IR32GBPS                 | Specified |
| PCIe 6.0   | Common clock         | PCIE6_T_RMSSC-REFCLK     | Specified |
|            |                      | PCIE6_T-WST-RMSSC-REFCLK | Specified |
|            | Independent RefClock | IR64GBPS                 | Specified |

### Supported AC Reference Clock measurements

#### AC Reference Clock specifications

PCIe TekExpress runs AC Reference Clock measurement using Skyworks Clock Jitter tool and additionally reports:

- Ring Back Voltage
- Overshoot Voltage relative to V(IH)
- Undershoot Voltage relative to V(IL)

| Generation                    | Specifications                    | Measurements                                                       | Symbol            |
|-------------------------------|-----------------------------------|--------------------------------------------------------------------|-------------------|
| Common across all generations | AC Reference Clock specifications | Cycle to Cycle jitter                                              | CC_JITTER         |
|                               |                                   | Differential Input High Voltage                                    | V_IH              |
|                               |                                   | Differential Input Low Voltage                                     | V_IL              |
|                               |                                   | Duty Cycle                                                         | Duty Cycle        |
|                               |                                   | Absolute Max input voltage                                         | V <sub>max</sub>  |
|                               |                                   | Absolute Min input voltage                                         | V <sub>min</sub>  |
|                               |                                   | Absolute Period (including Jitter and Spread Spectrum modulation)  | Period Abs        |
|                               |                                   | Falling Edge Rate                                                  | Falling-Edge-Rate |
|                               |                                   | Rising Edge Rate                                                   | Rising-Edge-Rate  |
|                               |                                   | Average Clock Period Accuracy                                      | Avg Prd Accur     |
|                               |                                   | Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching | Rise fall Match   |
|                               |                                   | Absolute crossing point voltage                                    | VCROSS            |
|                               |                                   | SSC SlewRate                                                       | SSC SlewRate      |

#### PCIe 7.0 Base transmitter measurements

| TX Test                           | Pattern                                            | Notes                                                    |
|-----------------------------------|----------------------------------------------------|----------------------------------------------------------|
| SNDR                              | Compliance                                         | Signal Noise Distortion Ratio                            |
| Voltage Differential Peak-to-Peak | Compliance                                         | Measured with 64 level 3s & 64 level 0s                  |
| Transmit Equalization             | Compliance                                         | Q0-Q10 (PAM4) with AC step method                        |
| Tx Equalization Boost             | Compliance                                         | Q10 (full swing) & Q4 (reduced swing)                    |
| EIEOS Min Voltage Swing           | Compliance                                         | Include package loss impact                              |
| Ratio Level Mismatch              | Compliance                                         | PAM4 measurement only                                    |
| Uncorrelated Tj                   | Toggle patterns of all twelve types of transitions | Jitter computed on each unique transition.               |
| Uncorrelated Dj_dd                |                                                    | Toggle Patterns: HSTP, LSTPO, LSTP1, LSTP2, LSTP3, LSTP4 |
| Random Jitter                     |                                                    | Informative                                              |

| TX Test                  | Pattern           | Notes                                   |
|--------------------------|-------------------|-----------------------------------------|
| Pulse Width Jitter TJ    | High Swing Toggle | 0303 level pattern; noise comp included |
| Pulse Width Jitter Dj_dd | High Swing Toggle | 0303 level pattern; noise comp included |
| PS21                     | Compliance        | Pseudo package loss                     |

**Signal Quality measurements included in Tektronix Option PCE7 (PCIe Gen 7.0)**

| Measurement Name            | PAMJET Measurement                                             | Limits                                     |
|-----------------------------|----------------------------------------------------------------|--------------------------------------------|
| RLM                         | RLM (PCIe)                                                     | 95% (min)                                  |
| SNDR                        | SNDR (PCIe)<br>Pmax (PCIe)<br>sigma_e (PCIe)<br>sigma_n (PCIe) | 34 dB (min)                                |
| Uncorrelated TIE TJ@E-06    | TTX-uTJ (PCIe)                                                 | 2 ps (max) @ BER E-6                       |
| Uncorrelated TIE DJ dd@E-06 | TTX-uDJDD (PCIe)                                               | 0.75 ps (max)                              |
| TIE RJ (RMS)                | TTX-RJ (PCIe)                                                  | 0.13 ps to 0.21 ps Informative             |
| Uncorrelated PWJ TJ@E-06    | TTX-UPW-TJ (PCIe)                                              | 2 ps (max) @ BER E-6                       |
| Uncorrelated PWJ DJ dd@E-06 | TTX-UPW-DJDD (PCIe)                                            | 0.625 ps (max)                             |
| PS21 Ratio                  | ps21TX                                                         | 8.5 dB max (Root)<br>3.7 dB max (Non-root) |
| AC CM 32 GHz                | VTX-ACCM-PP                                                    | 75 mV (max)                                |
| AC CM 30 kHz-500 MHz        | VTX-ACCM-PP-FILT                                               | 25 mV (max)                                |
| Unit Interval               |                                                                | 15.623438 ps to 15.626563 ps               |
| V Tx Diff Pk To Pk          | VTX-DIFF-PP                                                    | 800–1000 mV (Full), 400–1000 mV (Reduce)   |
| V Tx EIEOS                  | VTX-EIEOS                                                      | 250 mV min (Full), 232 mV min (Reduce)     |
| Tx Equalization Presets     | Tx Preset Equalization                                         | Table                                      |

**Tx preset ratios and corresponding coefficient values for 64 GT/s and 128 GT/s**

| Preset # | Preshoot 2 (dB) | Preshoot 1 (dB) | De-emphasis (dB) | C-2   | C-1    | C+1   | Va/Vd | Vb/Vd | Vc1/Vd | Vc2/Vd |
|----------|-----------------|-----------------|------------------|-------|--------|-------|-------|-------|--------|--------|
| Q0       | 0.0±0.5         | 0.0±0.5         | 0.0±0.5          | 0.000 | 0.000  | 0.000 | 1.000 | 1.000 | 1.000  | 1.000  |
| Q1       | 0.0±0.5         | 1.6±0.5         | 0.0±0.5          | 0.000 | -0.083 | 0.000 | 0.835 | 0.834 | 1.000  | 0.834  |
| Q2       | 0.0±0.5         | 3.5±0.5         | 0.0±0.5          | 0.000 | -0.167 | 0.000 | 0.666 | 0.666 | 1.000  | 0.666  |

| Preset # | Preshoot 2 (dB) | Preshoot 1 (dB) | De-emphasis (dB) | C-2   | C-1    | C+1    | Va/Vd | Vb/Vd  | Vc1/Vd | Vc2/Vd |
|----------|-----------------|-----------------|------------------|-------|--------|--------|-------|--------|--------|--------|
| Q3       | 0.0±0.5         | 0.0±0.5         | -1.6±0.5         | 0.000 | 0.000  | -0.083 | 1.000 | 0.834  | 0.834  | 0.834  |
| Q4       | 0.0±0.5         | 0.0±0.5         | -3.5±0.5         | 0.000 | 0.000  | -0.167 | 1.000 | 0.666  | 0.666  | 0.666  |
| Q5       | -1.3±0.5        | 4.7±1.0         | 0.0±0.5          | 0.042 | -0.208 | 0.000  | 0.584 | 0.584  | 1.000  | 0.500  |
| Q6       | -1.6±0.5        | 3.5±0.5         | -3.5±0.5         | 0.042 | -0.125 | -0.125 | 0.750 | 0.500  | 0.750  | 0.416  |
| Q7       | -2.9±0.5        | 4.7±1.0         | 0.0±0.5          | 0.083 | -0.208 | 0.000  | 0.584 | 0.584  | 1.000  | 0.418  |
| Q8       | -3.5±0.5        | 6.0±1.0         | 0.0±0.5          | 0.083 | -0.250 | 0.000  | 0.500 | 0.500  | 1.000  | 0.334  |
| Q9       | -4.4±1.0        | 6.9±1.0         | -1.6±0.5         | 0.083 | -0.250 | -0.042 | 0.500 | 0.416  | 0.916  | 0.250  |
| Q10      | 0.0±0.5         | 0.0±0.5         | Note 2           | 0.000 | 0.000  | Note 2 | 1.000 | Note 2 | Note 2 | Note 2 |

- Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
- Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training.

#### PCIe 6.0 Base and CEM transmitter measurements

| TX test                           | Pattern                 | Notes                                     |
|-----------------------------------|-------------------------|-------------------------------------------|
| SNDR                              | Compliance              | Signal Noise Distortion Ratio             |
| Voltage Differential Peak-to-Peak | Compliance              | Measured with 64 levels 3s & 64 level 0s  |
| Transmit Equalization             | Compliance              | Q0-Q10 (PAM4) with AC step method         |
| Tx Equalization Boost             | Compliance              | Q10 (full swing) & Q4 (reduced swing)     |
| EIEOS min Voltage Swing           | Compliance              | Include package loss impact               |
| Ratio Level Mismatch              | Compliance              | PAM4 measurement only                     |
| Uncorrelated Tj                   | 52UI Jitter Measurement | Jitter computed on each unique transition |
| Uncorrelated Dj                   | 52UI Jitter Measurement | Jitter computed on each unique transition |
| Uncorrelated Dj                   | 52UI Jitter Measurement | Informative                               |
| Pulse Width Jitter Tj             | High Swing Toggle       | 0303 level pattern; noise comp included   |
| Pulse Width Jitter Dj_dd          | High Swing Toggle       | 0303 level pattern; noise comp included   |
| Pulse Width Jitter Rj             | High Swing Toggle       | Informative                               |
| PS21                              | Compliance              | Pseudo package loss                       |

**Signal quality measurements included in Tektronix Option PCE6 (PCIe Gen 6.0)**

| Measurements                | Base Tx Test Board Gen 6.0 | Add-In Card Gen 6.0 | System Board Gen 6.0 |
|-----------------------------|----------------------------|---------------------|----------------------|
| UnitInterval                | ✓                          |                     |                      |
| AC_CM 16 GHz                | ✓                          |                     |                      |
| AC_CM 30 KHz-500 MHz        | ✓                          |                     |                      |
| PS21 Ratio                  | ✓                          |                     |                      |
| VTx_EIEOS                   | ✓                          |                     |                      |
| VTx_Diff_pk_To_Diff_pk      | ✓                          |                     |                      |
| VTx_Boost                   | ✓                          |                     |                      |
| Uncorrelated TIE TJ@E-06    | ✓                          | ✓                   |                      |
| Uncorrelated TIE DJ DD@E-06 | ✓                          | ✓                   |                      |
| Uncorrelated PWJ TJ@E-06    | ✓                          | ✓                   |                      |
| Uncorrelated PWJ DJ DD@E-06 | ✓                          | ✓                   |                      |
| TIE RJ (RMS)                | ✓                          | ✓                   |                      |
| SNDR                        | ✓                          | ✓                   |                      |
| RLM                         | ✓                          | ✓                   | ✓                    |
| EyeHeight                   |                            | ✓                   | ✓                    |
| EyeWidth                    |                            | ✓                   | ✓                    |

| Parameter                  | PAMJET measurement              | 64 GT/s Limit Rev 1.0                |
|----------------------------|---------------------------------|--------------------------------------|
| SNDR                       | SNDR (PCIe)                     | 34 dB (min)                          |
| RLM                        | R <sub>LM</sub> (PCIe)          | 95% (min)                            |
| Uncorrelated Jitter TJ     | T <sub>TX-uTJ</sub> (PCIe)      | 4.00 ps @ E-6 (max)                  |
| Uncorrelated Jitter Dj-dd  | T <sub>TX-uDJDD</sub> (PCIe)    | 1.563 ps @ E-6 (max)                 |
| Uncorrelated Jitter Rj     | T <sub>TX-uRJ</sub> (PCIe)      | Informative                          |
| Pulse Width Jitter TJ      | T <sub>TX-UPW-TJ</sub> (PCIe)   | 4.00 ps @ E-6 (max)                  |
| Pulse Width Jitter Dj-dd   | T <sub>TX-UPW-DJDD</sub> (PCIe) | 1.25 ps                              |
| Pulse Width Jitter Rj      | T <sub>TX-UPW-RJ</sub> (PCIe)   | Informative                          |
| Tx Preset Test (Q0 to Q10) | Tx Preset Equalization          | See the Tx preset ratios table below |

**Tx preset ratios and corresponding coefficient values for 64 GT/s and 128 GT/s**

| Preset # | Preshoot 2 (dB) | Preshoot 1 (dB) | De-emphasis (dB) | c <sub>-2</sub> | c <sub>-1</sub> | c <sub>+1</sub> | Va/Vd  | Vb/Vd  | Vc1/Vd | Vc2/Vd |
|----------|-----------------|-----------------|------------------|-----------------|-----------------|-----------------|--------|--------|--------|--------|
| Q0       | 0.0 ± 0.5       | 0.0 ± 0.5       | 0.0 ± 0.5        | 0.000           | 0.000           | 0.000           | 1.000  | 1.000  | 1.000  | 1.000  |
| Q1       | 0.0 ± 0.5       | -1.6 ± 0.5      | 0.0 ± 0.5        | 0.000           | 0.083           | 0.000           | 0.834  | 0.834  | 1.000  | 0.834  |
| Q2       | 0.0 ± 0.5       | 3.5 ± 0.5       | 0.0 ± 0.5        | 0.000           | 0.167           | 0.000           | 1.000  | 0.834  | 0.834  | 0.834  |
| Q3       | 0.0 ± 0.5       | 0.0 ± 0.5       | -1.6 ± 0.5       | 0.000           | 0.000           | -0.083          | 1.000  | 0.834  | 0.834  | 0.834  |
| Q4       | 0.0 ± 0.5       | 0.0 ± 0.5       | -3.5 ± 0.5       | 0.000           | 0.000           | -0.167          | 1.000  | 1.666  | 1.666  | 1.666  |
| Q5       | -1.3 ± 0.5      | 4.7 ± 1.0       | 0.0 ± 0.5        | 0.042           | -0.208          | 0.000           | 0.0584 | 0.0584 | 1.000  | 1.500  |
| Q6       | -1.6 ± 0.5      | 3.5 ± 0.5       | -3.5 ± 0.5       | 0.042           | -0.125          | -0.125          | 0.750  | 1.500  | 0.750  | 0.416  |
| Q7       | 2.9 ± 0.5       | 4.7 ± 1.0       | 0.0 ± 0.5        | 0.083           | -0.208          | 0.000           | 0.0584 | 0.0584 | 1.000  | 0.418  |
| Q8       | 3.5 ± 0.5       | 6.0 ± 1.0       | 0.0 ± 0.5        | 0.083           | -0.250          | 0.000           | 0.500  | 0.500  | 1.000  | 0.334  |
| Q9       | -4.4 ± 1.0      | 6.9 ± 1.0       | -1.6 ± 0.5       | 0.083           | -0.250          | 0.042           | 0.500  | 0.416  | 0.916  | 0.250  |
| Q10      | 0.0 ± 0.5       | 0.0 ± 0.5       | Note 2           | 0.000           | 0.000           | Note 2          | 1.000  | Note 2 | Note 2 | Note 2 |

**Supported PCIe 4.0 Base transmitter measurements**

| Parameter                                     | DPOJET measurement | 8 GT/s, Rev 3.0 | 16 GT/s, Rev 1.0 |
|-----------------------------------------------|--------------------|-----------------|------------------|
| Full Swing Tx voltage with noTxEq             | V-TX-FS-NO-EQ      | Specified       | Specified        |
| Reduced Swing Tx voltage with noTxEq          | V-TX-RS-NO-EQ      | Specified       | Specified        |
| Min swing during EIEOS for full swing         | V-TX-EIEOS-FS      | Specified       | Specified        |
| Min swing during EIEOS for reduced swing      | V-TX-EIEOS-RS      | Specified       | Specified        |
| Pseudo package loss Root device               | ps21TXRootdevice   | Specified       | Specified        |
| Pseudo package loss AIC device                | ps21TXAICdevice    | Specified       | Specified        |
| Tx uncorrelated total Jitter                  | T-TX-UTJ           | Specified       | Specified        |
| Tx uncorrelated deterministic jitter          | T-TX-UDJDD         | Specified       | Specified        |
| Data dependent jitter                         | T-TX-DDJ           | Specified       | Specified        |
| Total uncorrelated PWJ                        | T-TX-UPW-TJ        | Specified       | Specified        |
| Deterministic DjDD uncorrelated PWJ           | T-TX-UPW-DJDD      | Specified       | Specified        |
| Maximum Boost voltage ratio for full swing    | V-TX-FS-BOOST      | Specified       | Specified        |
| Maximum Boost voltage ratio for reduced swing | V-TX-RS-BOOST      | Specified       | Specified        |
| Tx DC peak-peak common mode voltage           | VTX_DC_CM          | Specified       | NA               |

| Parameter                                                  | DPOJET measurement   | 8 GT/s, Rev 3.0 | 16 GT/s, Rev 1.0 |
|------------------------------------------------------------|----------------------|-----------------|------------------|
| Absolute Delta of DC Common Mode Voltage between D+ and D- | VTX_CM_DC_LINE_DELTA | Specified       | NA               |
| Electrical Idle Differential Peak Output Voltage           | VTX_IDLE_DIFF_AC_p   | Specified       | NA               |
| DC Electrical Idle Differential Output Voltage             | VTX_IDLE_DIFF_DC     | Specified       | NA               |

## Supported PCIe 5.0 Base transmitter measurements

| Parameter                                        | DPOJET measurement | 32 GT/s, Rev 5.0                |
|--------------------------------------------------|--------------------|---------------------------------|
| Tx uncorrelated total Jitter                     | T-TX-UTJ           | 6.25 ps (max)                   |
| Tx uncorrelated deterministic Jitter             | T-TX-UDJDD         | 3.125 ps (max)                  |
| Data dependent Jitter                            | T-TX-DDJ           | NA                              |
| Total uncorrelated PWJ                           | T-TX-UPW-TJ        | 6.25 ps (max)                   |
| Total Random Jitter (informative)                | T-TX-RJ            | 0.23-0.45 ps rms                |
| Deterministic DjDD uncorrelated PWJ              | T-TX-UPW-DJDD      | 2.5 ps (max)                    |
| RMS RefClk jitter for common RefClk architecture | T-RMSCC-RCLK       | 0.25 ps (max)                   |
| IR RefClk jitter                                 | IR32GBPS           | NA                              |
| Pseudo Package Loss                              | ps21Tx             | (max) 8.5dB                     |
| Boost ratio                                      | VTX-BOOST          | 8.0 (min) dB                    |
| EIEOS                                            | VTX-EIEOS          | 250 mV                          |
| TX Differential Peak to Peak                     | VTX-DIFF-PP        | 800 mV (max) 1300mV             |
| Unit Interval                                    | UI                 | 31.246875 (min) 31.253125 (max) |

## Differential transmitter output measurements

| Parameter                                            | Symbol(s)                                 | 2.5 GT/s Rev 1.1/2.0 | 5 GT/s Rev 2.0 |
|------------------------------------------------------|-------------------------------------------|----------------------|----------------|
| Clock Recovery                                       | NA                                        | Specified            | Specified      |
| Unit Interval                                        | UI                                        | Specified            | Specified      |
| Differential Peak-to-Peak Tx Voltage Swing           | VTX-DIFF-P-P<br>VTX-SWING<br>VTX-EYE-FULL | Specified            | Specified      |
| Low-power Differential Peak-to-Peak Tx Voltage Swing | VTX-SWING-LOW<br>VTX-EYE-HALF             | Specified            | Specified      |
| De-emphasized Output Voltage Ratio                   | VTX-DE-RATIO                              | Not Specified        | Specified      |

| Parameter                                                                    | Symbol(s)                                     | 2.5 GT/s Rev 1.1/2.0 | 5 GT/s Rev 2.0 |
|------------------------------------------------------------------------------|-----------------------------------------------|----------------------|----------------|
| Instantaneous Lane Pulse Width                                               | T <sub>MIN-PULSE</sub>                        | Not Specified        | Specified      |
| Transmitter Eye including All Jitter Sources                                 | T <sub>TX-EYE</sub><br>T <sub>TX-EYE-TJ</sub> | Specified            | Specified      |
| Maximum Time between the Jitter Median and Maximum Deviation from the Median | T <sub>TX-EYEMEDIAN-to-MAXJITTER</sub>        | Specified            | Specified      |
| Deterministic Jitter                                                         | T <sub>TX-DJ-DD</sub>                         | Not Specified        | Specified      |
| Tx RMS Jitter <1.5 MHz                                                       | T <sub>TX-LF-RMS</sub>                        | Not Specified        | Specified      |
| D+/D– Tx Output Rise/Fall Time                                               | T <sub>TX-RISE</sub><br>T <sub>TX-FALL</sub>  | Specified            | Specified      |
| Tx Rise/Fall Mismatch                                                        | T <sub>RF-MISMATCH</sub>                      | Not Specified        | Specified      |
| AC Peak-to-Peak Common Mode Output Voltage                                   | V <sub>TX-CM-AC-PP</sub>                      | Not Specified        | Specified      |
| AC Peak Common Mode Output Voltage                                           | V <sub>TX-CM-AC-P</sub>                       | Specified            | Specified      |
| Absolute Delta of DC Common Mode Voltage between D+ and D–                   | V <sub>TX-CM-DC-LINE-DELTA</sub>              | Specified            | Specified      |

## Supported CEM specification measurements

### Add-in Card 8 GT/s transmitter path compliance measurements

| Parameter                 | Symbol       |
|---------------------------|--------------|
| Transition Eye Voltage    | PCIe V-TXA   |
| Nontransition Eye Voltage | PCIe V-TXA-d |
| Eye Width                 | PCIe T-TXA   |

### Add-in Card transmitter path compliance measurements

| Parameter                                        | Symbol(s)                   | 2.5 GT/s Rev 1.1/2.0 | 5 GT/s Rev 2.0 |
|--------------------------------------------------|-----------------------------|----------------------|----------------|
| Clock Recovery                                   | NA                          | Specified            | Specified      |
| Unit Interval                                    | UI                          | Specified            | Specified      |
| Eye Height of Transition Bits                    | V <sub>TXA</sub>            | Specified            | Specified      |
| Eye Height of Nontransition Bits                 | V <sub>TXA_d</sub>          | Specified            | Specified      |
| Eye Width with Sample Size of 10 <sup>6</sup> UI | T <sub>TXA</sub> in Rev 1.1 | Specified            | Not Specified  |
| Jitter Eye Opening at BER 10 <sup>–12</sup>      | T <sub>TXA</sub> in Rev 2.0 | Specified            | Specified      |

| Parameter                                                       | Symbol(s)                             | 2.5 GT/s Rev 1.1/2.0 | 5 GT/s Rev 2.0 |
|-----------------------------------------------------------------|---------------------------------------|----------------------|----------------|
| Maximum Median-Max Jitter Outlier with Sample Size of $10^6$ UI | J <sub>TXA-MEDIAN-to-MAX-JITTER</sub> | Specified            | Not Specified  |
| Total Jitter at BER $10^{-12}$                                  | TJ at BER $10^{-12}$                  | Not Specified        | Specified      |
| Deterministic Jitter at BER $10^{-12}$                          | Max DJ                                | Not Specified        | Specified      |

#### System board transmitter path measurements

| Parameter                                                       | Symbol(s)                             | 2.5 GT/s Rev 1.1/2.0 | 5 GT/s Rev 2.0 |
|-----------------------------------------------------------------|---------------------------------------|----------------------|----------------|
| Clock Recovery                                                  | NA                                    | Specified            | Specified      |
| Unit Interval                                                   | UI                                    | Specified            | Specified      |
| Eye Height of Transition Bits                                   | V <sub>TXS</sub>                      | Specified            | Specified      |
| Eye Height of Nontransition Bits                                | V <sub>TXS_d</sub>                    | Specified            | Specified      |
| Eye Width with Sample Size of $10^6$ UI                         | T <sub>TXS</sub> in Rev 1.1           | Specified            | Not Specified  |
| Jitter Eye Opening at BER $10^{-12}$                            | T <sub>TXS</sub> in Rev 2.0           | Specified            | Specified      |
| Maximum Median-Max Jitter Outlier with Sample Size of $10^6$ UI | J <sub>TXA-MEDIAN-to-MAX-JITTER</sub> | Specified            | Not Specified  |
| Total Jitter at BER $10^{-12}$                                  | TJ at BER $10^{-12}$                  | Not Specified        | Specified      |
| Deterministic Jitter at BER $10^{-12}$                          | Max DJ                                | Not Specified        | Specified      |

#### Reference Clock measurements

| Parameter                                     | Symbol | 2.5 GT/s Rev 1.1/2.0 |
|-----------------------------------------------|--------|----------------------|
| Reference Clock Phase Jitter at BER $10^{-6}$ | NA     | Specified            |

#### PCIe Module™ measurements

##### ExpressModule Add-in Card transmitter path measurements

| Parameter                               | Symbol                      | Rev 1.0   |
|-----------------------------------------|-----------------------------|-----------|
| Clock Recovery                          | NA                          | Specified |
| Unit Interval                           | UI                          | Specified |
| Eye Height of Transition Bits           | V <sub>TXA</sub>            | Specified |
| Eye Height of Nontransition Bits        | V <sub>TXA_d</sub>          | Specified |
| Eye Width with Sample Size of $10^6$ UI | T <sub>TXA</sub> in Rev 1.1 | Specified |
| Jitter Eye Opening at BER $10^{-12}$    | NA                          | Specified |

| Parameter                                                       | Symbol                                | Rev 1.0   |
|-----------------------------------------------------------------|---------------------------------------|-----------|
| Maximum Median-Max Jitter Outlier with Sample Size of $10^6$ UI | J <sub>TXA-MEDIAN-to-MAX-JITTER</sub> | Specified |

#### ExpressModule system board transmitter path measurements

| Parameter                                                       | Symbol                                | Gen 1.0 Rev 1.0 |
|-----------------------------------------------------------------|---------------------------------------|-----------------|
| Clock Recovery                                                  | NA                                    | Specified       |
| Unit Interval                                                   | UI                                    | Specified       |
| Eye Height of Transition Bits                                   | V <sub>TXS</sub>                      | Specified       |
| Eye Height of Nontransition Bits                                | V <sub>TXS_d</sub>                    | Specified       |
| Eye Width with Sample Size of $10^6$ UI                         | T <sub>TXS</sub>                      | Specified       |
| Jitter Eye Opening at BER $10^{-12}$                            | NA                                    | Specified       |
| Maximum Median-Max Jitter Outlier with Sample Size of $10^6$ UI | J <sub>TXA-MEDIAN-to-MAX-JITTER</sub> | Specified       |

#### PCIe external cabling measurements

##### External cabling transmitter path measurements

| Parameter                               | Symbol                 | Rev 1.0   |
|-----------------------------------------|------------------------|-----------|
| Clock Recovery                          | NA                     | Specified |
| Unit Interval                           | UI                     | Specified |
| Eye Height of Transition Bits           | V <sub>TXA</sub>       | Specified |
| Eye Height of Nontransition Bits        | V <sub>TXA_d</sub>     | Specified |
| Jitter Eye Opening at BER $10^{-12}$    | TrxA at BER $10^{-12}$ | Specified |
| Eye Width with Sample Size of $10^6$ UI | TrxA at $10^6$ Samples | Specified |

#### PCMCIA ExpressCard™ measurements

##### ExpressCard - Module transmitter path measurements

| Parameter                        | Symbol             | Release 1.0 |
|----------------------------------|--------------------|-------------|
| Clock Recovery                   | NA                 | Specified   |
| Unit Interval                    | UI                 | Specified   |
| Eye Height of Transition Bits    | V <sub>TXA</sub>   | Specified   |
| Eye Height of Nontransition Bits | V <sub>TXA_d</sub> | Specified   |
| Eye Width across any 250 UIs     | T <sub>TXA</sub>   | Specified   |

### ExpressCard - Host system transmitter path measurements

| Parameter                        | Symbol       | Release 1.0 |
|----------------------------------|--------------|-------------|
| Clock Recovery                   | NA           | Specified   |
| Unit Interval                    | UI           | Specified   |
| Eye Height of Transition Bits    | $V_{txS}$    | Specified   |
| Eye Height of Nontransition Bits | $V_{txS\_d}$ | Specified   |
| Eye Width across any 250 UIs     | $T_{TxS}$    | Specified   |

### MXM measurements

All de-emphasis levels supported

### PCIe measurements

| Parameter                        | Symbol       | Release 1.1 |
|----------------------------------|--------------|-------------|
| Eye Height of Transition Bits    | $V_{TXS}$    | Specified   |
| Eye Height of Nontransition Bits | $V_{TXS\_d}$ | Specified   |
| Width at BER                     | $T_{TXS}$    | Specified   |
| Deterministic Jitter             | DJ           | Specified   |
| Total Jitter                     | TJ           | Specified   |

## Ordering information

### To order on 7 Series oscilloscope, model DP0714AX (for PCIe Gen 1-4):

| Nomenclature                                                                                                                                                | Description                                                                                                                                                                     |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>7 Series DPO &gt;= 8 GHz</b> (bandwidth requirements vary for specific generations. Refer to the recommended oscilloscopes section for more information) |                                                                                                                                                                                 |
| 7-CMPCIE1234                                                                                                                                                | License; PCIe Gen1.0 Gen 2.0 Gen 3.0 Gen 4.0 Tx Automated Compliance Solution using TekExpress Framework; Canned, Electronically Downloaded; Requires option 7-WIN; Node Locked |
| 7-CMPCIE1234-FL                                                                                                                                             | License; PCIe Gen1.0 Gen 2.0 Gen 3.0 Gen 4.0 Tx Automated Compliance Solution using TekExpress Framework; Canned, Electronically Downloaded; Requires option 7-WIN; Floating    |

### To order switch matrix support on 7 Series oscilloscope, model DP0714AX:

| Nomenclature  | Description                                                                           |
|---------------|---------------------------------------------------------------------------------------|
| 7-SWX-PCIE-FL | License: Switch Matrix support for PCIe Tx; requires option 7-CMPCIE1234; Floating    |
| 7-SWX-PCIE    | License: Switch Matrix support for PCIe Tx; requires option 7-CMPCIE1234; Node Locked |

### To order on MSO/DP070000 DX/SX Series

#### SWX-PCE (requires option PCE3, 4 or 5)

Switch configurator for PCIe Gen 1.0/2.0/3.0/4.0/5.0

#### New instrument orders

Option SWX-PCE

#### Floating licenses

DPOFL-SWX-PCE

### Recommended MSO/DP070000 Series oscilloscopes

#### 2.5 Gb/s (PCIe 1.0/1.1)

7 Series scope, model DPO714AX, MSO70000 (6 GHz or higher bandwidth models required for compliance testing)

#### 5 Gb/s (PCIe 2.0)

7 Series scope, model DPO714AX, MSO70000 (12.5 GHz or higher bandwidth models)

#### 8 Gb/s (PCIe 3.0)

7 Series scope, model DPO714AX, MSO70000 (12.5 GHz or higher bandwidth models)

#### 16 Gb/s (PCIe 4.0)

7 Series scope, model DPO714AX, MSO70000 (25 GHz or higher bandwidth models)

#### 32 Gb/s (PCIe 5.0)

DPS77004SX Series (50 GHz or higher bandwidth models), MSO/DPO70000 Series (33 GHz or higher bandwidth models for Gen 5.0 CEM testing)

## 64 Gb/s (PCIe 6.0)

DPS77004SX Series (50 GHz or higher bandwidth models)

## 128 Gb/s (PCIe 7.0)

DPS77004SX Series (70 GHz bandwidth models)

## Supported DP070000 Series and 7 Series oscilloscope, model DP0714AX configurations

| Model            | Description                                                                                | Option PCE3 | Option PCE4 | Option PCE5 | Option PCE6 | Option PCE7 | Option CMPCIE1234        |
|------------------|--------------------------------------------------------------------------------------------|-------------|-------------|-------------|-------------|-------------|--------------------------|
| DPO73304DX       | 33 GHz DPO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s                                                | ✓           | ✓           | ✓           |             |             |                          |
| MSO72304DX       | 23 GHz MSO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s                                                | ✓           |             |             |             |             |                          |
| MSO72504DX       | 23 GHz MSO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s                                                | ✓           | ✓           |             |             |             |                          |
| MSO73304DX       | 33 GHz MSO; 2 Ch, 100 GS/s or 4 Ch, 50 GS/s                                                | ✓           | ✓           | ✓           |             |             |                          |
| DPO77002SX       | 70 GHz ATI; 1 Ch, 70 GHz, 200 GS/s or 2 Ch, 33GHz, 100 GS/s                                | ✓           | ✓           | ✓           |             |             |                          |
| DPS77004SX       | 70 GHz ATI System; 2 Ch: 70 GHz: 200 GS/s or 4Ch: 33 GHz: 100 GS/s                         | ✓           | ✓           | ✓           | ✓           | ✓           |                          |
| DPO75902SX       | 59 GHz ATI; 1 Ch, 59 GHz, 200 GS/s or 2 Ch, 33GHz, 100 GS/s                                | ✓           | ✓           | ✓           |             |             |                          |
| DPS75904SX       | 59 GHz ATI System; 2 Ch: 59 GHz: 200 GS/s or 4Ch: 33 GHz: 100 GS/s                         | ✓           | ✓           | ✓           | ✓           |             |                          |
| DPO75002SX       | 50 GHz ATI; 1 Ch, 50 GHz, 200 GS/s or 2 Ch, 33GHz, 100 GS/s                                | ✓           | ✓           | ✓           |             |             |                          |
| DPS75004SX       | 50 GHz ATI System; 2 Ch: 50 GHz: 200 GS/s or 4Ch: 33 GHz: 100 GS/s                         | ✓           | ✓           | ✓           | ✓           |             |                          |
| DPO73304SX       | 33 GHz DPO; 2 Ch, 33 GHz, 100 GS/s or 4 Ch, 23 GHz, 50 GS/s                                | ✓           | ✓           | ✓           |             |             |                          |
| DPS73308SX       | 33 GHz DPO System; 4 Ch: 33 GHz: 100 GS/s or 4 Ch: 23 GHz: 50 GS/s                         | ✓           | ✓           | ✓           |             |             |                          |
| DPO714AX (8 GHz) | 8 GHz bandwidth, (4) TekConnect Channels with 125 GS/S sample rate and 500 M record length |             |             |             |             |             | ✓ (support Gen 1.0 only) |

| Model                | Description                                                                                 | Option PCE3 | Option PCE4 | Option PCE5 | Option PCE6 | Option PCE7 | Option CMPCIE1234                           |
|----------------------|---------------------------------------------------------------------------------------------|-------------|-------------|-------------|-------------|-------------|---------------------------------------------|
| DPO714AX<br>(10 GHz) | 10 GHz bandwidth, (4) TekConnect Channels with 125 GS/S sample rate and 500 M record length |             |             |             |             |             | ✓ (supports Gen 1.0 and 2.0 only)           |
| DPO714AX<br>(13 GHz) | 13 GHz bandwidth, (4) TekConnect Channels with 125 GS/S sample rate and 500 M record length |             |             |             |             |             | ✓ (supports Gen 1.0, 2.0, and 3.0 only)     |
| DPO714AX<br>(16 GHz) | 16 GHz bandwidth, (4) TekConnect Channels with 125 GS/S sample rate and 500 M record length |             |             |             |             |             | ✓ (supports Gen 1.0, 2.0, and 3.0 only)     |
| DPO714AX<br>(20 GHz) | 20 GHz bandwidth, (4) TekConnect Channels with 125 GS/S sample rate and 500 M record length |             |             |             |             |             | ✓ (supports Gen 1.0, 2.0, 3.0 only)         |
| DPO714AX<br>(25 GHz) | 25 GHz bandwidth, (4) TekConnect Channels with 125 GS/S sample rate and 500 M record length |             |             |             |             |             | ✓ (supports Gen 1.0, 2.0, 3.0 and 4.0 only) |

## Recommended accessories

### P75xx, P76xx, and P77xx Series (TriMode™ Differential Probes)

| PCIe           |                                |                         |                          |                       |                       |                       |
|----------------|--------------------------------|-------------------------|--------------------------|-----------------------|-----------------------|-----------------------|
| Speed          | Minimum oscilloscope bandwidth | TCA-SMA<br>(Max 18 GHz) | TCA-292D<br>(Max 33 GHz) | P7500<br>(Max 20 GHz) | P7700<br>(Max 20 GHz) | P7600<br>(Max 33 GHz) |
| 2.5 GT/s       | 6 GHz                          | ✓                       | ✓                        | ✓                     | ✓                     | ✓                     |
| 5.0 GT/s       | 12.5 GHz                       | ✓                       | ✓                        | ✓                     | ✓                     | ✓                     |
| 8.0 GT/s       | 12.5 GHz                       | ✓                       | ✓                        | ✓                     | ✓                     | ✓                     |
| 16.0 GT/s      | 25 GHz                         |                         | ✓                        |                       |                       | ✓                     |
| 32.0 GT/s Base | 50 GHz                         |                         |                          |                       |                       |                       |
| 32.0 GT/s CEM  | 33 GHz                         |                         | ✓                        |                       |                       | ✓                     |
| 100 MHz RefClk | 5 GHz                          | ✓                       | ✓                        | ✓                     | ✓                     | ✓                     |

### Option SDLA64

Serial Data Link Analysis Visualizer. SDLA is not required for TekExpress automation solutions. It is mandatory for DPOJET PCIe.

### **Option SR-PCIe**

Bus decode support for PCIe serial busses. This is required to perform pattern decoding using TekExpress which gives Preset number and Lane number information (Only for Gen 3.0, currently Gen 4.0 is not supported). This feature is supported only for MSO/DPO70000 models.

### **Option PAMPCIE6**

Used for Gen 6.0 Base and CEM

### **Option PAMPCIE7**

Used for Gen 7.0 Base

## **Recommended for automated DUT control**

### **RF Switch**

Mini Circuits ZTM/ZTM2 40 GHz RF switch (Supports x4, x8, x16 configuration)

### **Tektronix AFG3252**

Arbitrary Function Generator

### **Tektronix AFG3252C**

Arbitrary Function Generator

### **AWG5002B/C**

Arbitrary Waveform Generator

### **AWG5012B/C**

Arbitrary Waveform Generator

### **AWG5014B/C**

Arbitrary Waveform Generator

### **AWG7082B/C**

Arbitrary Waveform Generator

### **AWG7122B/C**

Arbitrary Function Generator

### **AWG70001A**

Arbitrary Waveform Generator

### **AWG70002A**

Arbitrary Waveform Generator

### **AFG31252**

Arbitrary Function Generator

### **AFG31251**

Arbitrary Function Generator

## AFG3252C

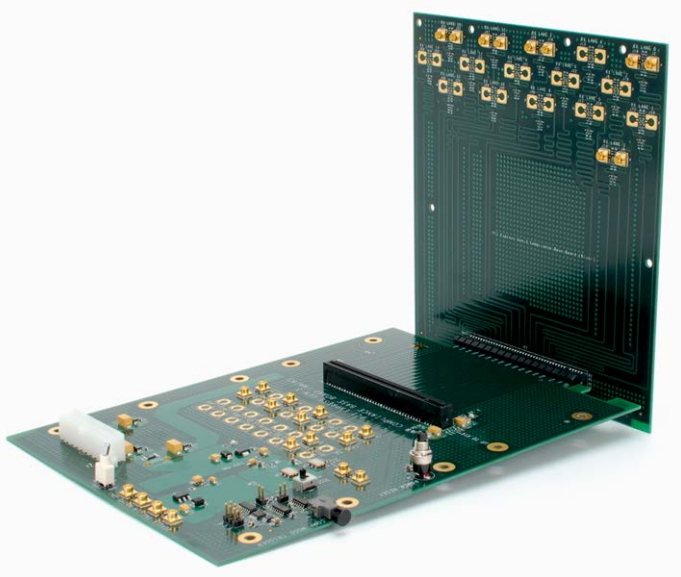
Arbitrary Function Generator

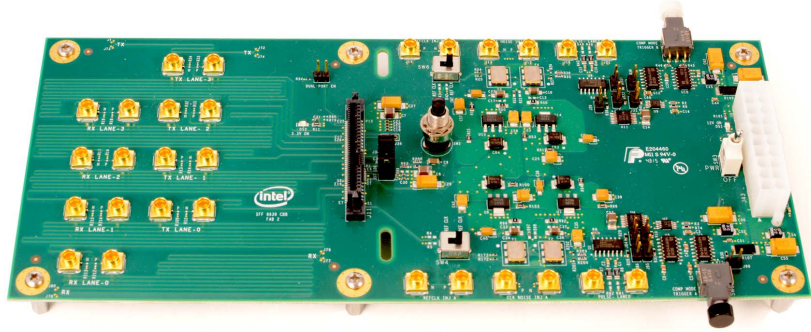
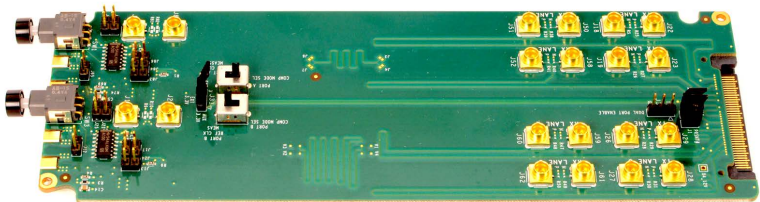
## GRL PCIE34 controller for automatic test pattern toggling and DUT power cycle (for Add-In-Card)

Part number : GRL-PCIE34-P1

Contact GRL at [support@graniteriverlabs.com](mailto:support@graniteriverlabs.com) for support and [quote@graniteriverlabs.com](mailto:quote@graniteriverlabs.com) to request for a quote.

## Recommended test fixtures, cables, and tools

| Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Image                                                                                |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| <p><b>Description:</b> [PCI-SIG] PCIe CEM 6.0 Test Fixture Kit</p> <p><b>Product Code:</b> CEM 6.0 Kit</p> <p>PCIe CEM 6.0 compliance load boards and baseboard designed for Tx/Rx validation with reuse of Gen5 ISI and cable infrastructure.</p> <p><b>Quantity:</b> 1</p> <p><a href="https://pcisig.com/specifications/fixture-order-form">https://pcisig.com/specifications/fixture-order-form</a></p>                                                                                                                      |                                                                                      |
| <p><b>Description:</b> [PCI-SIG] PCIe CEM 6.0 CBB/CLBs</p> <p><b>Product Code:</b> CEM 6.0 CBB/CLBs</p> <p>Complete PCIe CEM 6.0 test fixture kit enabling end-to-end transmitter and channel validation including ISI board and cables.</p> <p><b>Quantity:</b> 1</p> <p><a href="https://pcisig.com/specifications/fixture-order-form">https://pcisig.com/specifications/fixture-order-form</a></p>                                                                                                                            |                                                                                      |
| <p><b>Description:</b> [PCI-SIG] PCIe 4.0 CEM Fixture Kit</p> <p><b>PN:</b> PCIe-CLB-X1X16, PCIe-CLB-X4X8, PCIe-CBB-MAIN, and PCIe-VAR-ISI</p> <p>The PCIe 4.0 CEM Beta fixtures require a VNA based characterization to determine the appropriate Insertion Loss for performing the 16 GT/s Tx Signal Quality Test and the 16 GT/s Rx Link Equalization Test. This characterization will not be performed by the PCI-SIG, but must be performed by the end user after the fixtures are delivered.</p> <p><b>Quantity:</b> 1</p> |                                                                                      |
| <p><b>Description:</b> PCIe Compliance Base Board (CBB) test fixture, revision 3.0. For testing PCIe add-in cards, x1/x4/x8/x16 PCIe connectors on PCIe devices/add-in cards.</p> <p><b>Vendor:</b> PCI-SIG</p> <p><a href="https://pcisig.com/specifications/fixture-order-form">https://pcisig.com/specifications/fixture-order-form</a></p> <p><b>Vendor PN:</b> CBB3</p> <p><b>Tektronix PN:</b> Only available from PCI-SIG</p> <p><b>Quantity:</b> 1</p>                                                                   |  |

| Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Image                                                                                |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| <p><b>Description:</b> PCIe Compliance Load Board (CLB3) test fixture, revision 3.0. For testing PCIe Platforms, x1 and x16 PCIe connectors on PCIe systems/mother boards.</p> <p><b>Vendor:</b> PCI-SIG</p> <p><a href="https://pcisig.com/specifications/fixture-order-form">https://pcisig.com/specifications/fixture-order-form</a></p> <p><b>Vendor PN:</b> x1/x16 CLB3</p> <p><b>Tektronix PN:</b> Only available from PCI-SIG</p> <p><b>Quantity:</b> 1</p>                                                 |    |
| <p><b>Description:</b> PCIe Compliance Load Board (CLB3), Revision 3.0. For testing PCIe Platforms, x4 and x8 PCIe connectors on PCIe systems/mother boards.</p> <p><b>Vendor:</b> PCI-SIG</p> <p><a href="https://pcisig.com/specifications/fixture-order-form">https://pcisig.com/specifications/fixture-order-form</a></p> <p><b>Vendor PN:</b> x4/x8 CLB3</p> <p><b>Tektronix PN:</b> Only available from PCI-SIG</p> <p><b>Quantity:</b> 1</p>                                                                |    |
| <p><b>Description:</b> PCIe Compliance Load Board (U.2 CLB3) test fixture, revision 3.0. For testing PCIe Platforms, x1 and x4 PCIe connectors on PCIe devices/add-in cards.</p> <p><b>Vendor:</b> PCI-SIG</p> <p><a href="https://pcisig.com/specifications/fixture-order-form">https://pcisig.com/specifications/fixture-order-form</a></p> <p><b>Vendor PN:</b> U.2 CLB3</p> <p><b>Tektronix PN:</b> Only available from PCI-SIG</p> <p><b>Quantity:</b> 1</p> <p>Note: U.2 was formally known as SFF-8639.</p> |   |
| <p><b>Description:</b> PCIe Compliance Load Board (U.2 CLB3), Revision 3.0. For testing PCIe Platforms, x1 and x4 PCIe connectors on PCIe systems/mother boards.</p> <p><b>Vendor:</b> PCI-SIG</p> <p><a href="https://pcisig.com/specifications/fixture-order-form">https://pcisig.com/specifications/fixture-order-form</a></p> <p><b>Vendor PN:</b> U.2 CLB3</p> <p><b>Tektronix PN:</b> Only available from PCI-SIG</p> <p><b>Quantity:</b> 1</p> <p>Note: U.2 was formally known as SFF-8639.</p>             |  |

| Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Image                                                                                |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| <p><b>Description:</b> Any ATX PC power supply</p> <p><b>Vendor:</b> Tektronix recommends "PC Power and Cooling 750 W Silencer MK III Series" or similar.</p> <p><b>Quantity:</b> 1</p>                                                                                                                                                                                                                                                                                                                                                                                     |    |
| <p><b>Description:</b> SMP terminator, 50 <math>\Omega</math>, limited detent.</p> <p><b>Vendor:</b> Fairview Microwave</p> <p><a href="http://www.fairviewmicrowave.com/rf-load-0.25-watts-26.5-ghz-smp-female-st2645-p.aspx">http://www.fairviewmicrowave.com/rf-load-0.25-watts-26.5-ghz-smp-female-st2645-p.aspx</a></p> <p><b>Vendor PN:</b> ST2645</p> <p><b>Tektronix PN:</b> 131-9399-xx</p> <p><b>Quantity needed per PCIe DUT link width:</b></p> <ul style="list-style-type: none"> <li>▪ x1: 0</li> <li>▪ x4: 6</li> <li>▪ x8: 14</li> <li>▪ x16: 30</li> </ul> |   |
| <p><b>Description:</b> SMA Female to BNC Male adapter.</p> <p><b>Vendor:</b> Tektronix</p> <p><b>Tektronix PN:</b> 015-0572-xx</p> <p><b>Quantity:</b> 2</p>                                                                                                                                                                                                                                                                                                                                                                                                                |  |
| <p><b>Description:</b> DC Block, SMA, 26 GHz</p> <p><b>Vendor:</b> Tektronix</p> <p><b>Tektronix PN:</b> PSPL5500A, PSPL5501A, or PSPL5508</p> <p><b>Quantity:</b> 2</p> <p><b>Note:</b> This is an optional accessory and not shown in any of connection diagrams, but can be used if DC offset is encountered in any signal path.</p>                                                                                                                                                                                                                                     |  |

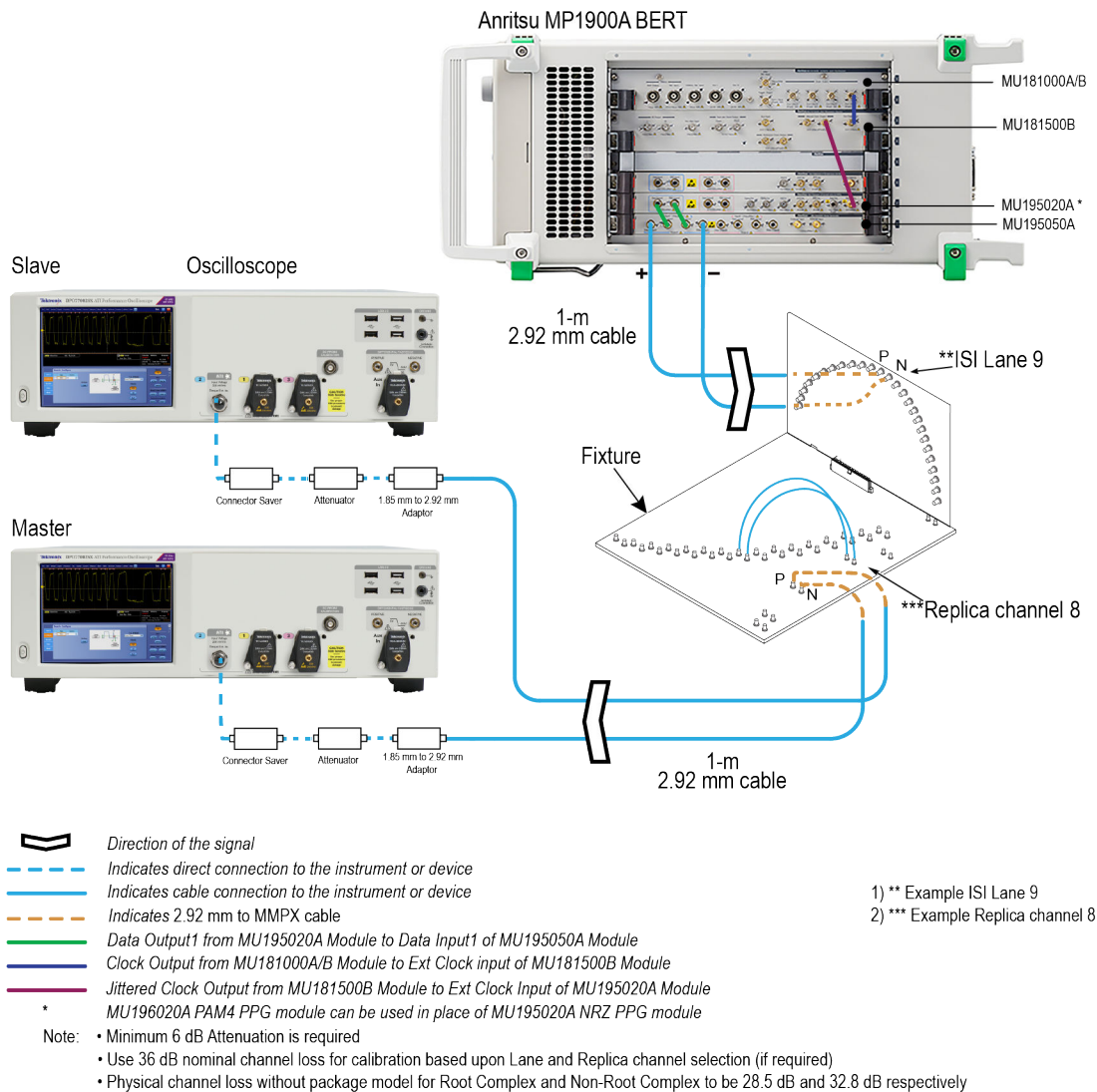
| Description                                                                                                                                                                                                                                       | Image                                                                                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| <p><b>Description:</b> USB2.0 Cable, Type A Male to Type B Male, 6 foot</p> <p><b>Vendor:</b> Tektronix</p> <p><b>Tektronix PN:</b> 174-6053-xx</p> <p><b>Quantity:</b> 1</p>                                                                     |    |
| <p><b>Description:</b> SMA-to-SMA, H+S SF104E Phase Kit (#84077556), Straight, 1`m, 1.5 ps phase-matched.</p> <p><b>Vendor:</b> Tektronix</p> <p><b>Tektronix PN:</b> PMCABLE1M</p> <p><b>Quantity:</b> 1 cable pair per lane</p>                 |  |
| <p><b>Description:</b> SMA-to-SMP right-angle cable pair, 102 mm, 1 ps phase-matched.</p> <p><b>Tektronix PN:</b> 174-6657-xx</p> <p><b>Quantity:</b> 1 cable pair</p> <p><b>Note:</b> Applicable only for Gen 3</p>                              |  |
| <p><b>Description:</b> SMA-to-SMP right-angle cable pair, 1 m, 1 ps phase-matched (one for AFG to Rx Lane0, one for 100 MHz RefClk for Ch3+4 for System Testing)</p> <p><b>Tektronix PN:</b> 174-6659-xx</p> <p><b>Quantity:</b> 1 cable pair</p> |  |

| Description                                                                                                                                                                                                                                                                                                                                                                                                    | Image                                                                                |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| <p><b>Description:</b> SMP to SMP right-angle cable pair, 305 mm, 2.5 ps phase-matched set.</p> <p><b>Tektronix PN:</b> 174-6658-xx</p> <p><b>Quantity:</b> 1 cable pair</p>                                                                                                                                                                                                                                   |    |
| <p><b>Description</b> Cables</p> <p><b>Tektronix PN</b> TF-PCIE5-CEM-X1 or TF-PCIE5-CEM-X16</p> <p><b>Specifications</b></p> <ul style="list-style-type: none"> <li>▪ Huber Suhner 24" MMPX PLUG to MMPX PLUG cable</li> <li>▪ PN 174-7327-00</li> <li>▪ QTY = 4</li> <li>▪ Huber Suhner 4" MMPX – 2.92 Cable 32024E-29430CR-29092KCR-24PM +/-1 PS-STD</li> <li>▪ PN 174-7326-00</li> <li>▪ QTY = 4</li> </ul> |                                                                                      |
| <p><b>Description:</b> SMA torque wrench, 8.0 in-lbs.</p> <p><b>Vendor:</b> Fairview Microwave</p> <p><a href="http://www.fairviewmicrowave.com/sma-fixed-torque-wrench-click-st-sma3-p.aspx">http://www.fairviewmicrowave.com/sma-fixed-torque-wrench-click-st-sma3-p.aspx</a></p> <p><b>Vendor PN:</b> ST-SMA3</p> <p><b>Tektronix PN:</b> 003-1940-xx</p> <p><b>Quantity:</b> 1</p>                         |  |
| <p><b>Description:</b> SMP right-angle cable extraction tool.</p> <p><b>Vendor:</b> Fairview Microwave</p> <p><a href="http://www.fairviewmicrowave.com/undefined-mmtl2682-p.aspx">http://www.fairviewmicrowave.com/undefined-mmtl2682-p.aspx</a></p> <p><b>Vendor PN:</b> MMTL2682</p> <p><b>Tektronix PN:</b> 003-1941-xx</p> <p><b>Quantity:</b> 1</p>                                                      |  |

| Description                                                                                                                                                                                                                                                                                                                                                     | Image                                                                              |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|
| <p><b>Description:</b> SMP terminator installation/extraction tool.</p> <p><b>Vendor:</b> Fairview Microwave</p> <p><a href="http://www.fairviewmicrowave.com/undefined-mmtl4991-p.aspx">http://www.fairviewmicrowave.com/undefined-mmtl4991-p.aspx</a></p> <p><b>Vendor PN:</b> MMTL4991</p> <p><b>Tektronix PN:</b> 003-1939-xx</p> <p><b>Quantity:</b> 1</p> |  |

## PCIe receiver testing

Tektronix also offers a PCIe receiver testing solution from PCIe Gen 1.0 to Gen 7.0 that includes stressed pattern generation as required by PCI-SIG test specifications and support for automated calibration and receiver tests. Automated DUT loopback control simplifies the testing process and reduces the time to test results. For more information, refer to the [PCIe Rx datasheet](#).



1620-005

### PCIe receiver test setup

Salient features of the Receiver automation software with Tektronix DPO70000SX Series Real-Time Scopes and Anritsu MP1900A BERT are as follows:

- Wizard-based user interface for each step of calibration and test
- Efficient and quick calibration
- Insertion Loss computation powered by Seasim Statistical Simulation Tool
- Tx Link Equalization/Rx Link Equalization
- Jitter Tolerance

- Latest industry tool support (SigTest and Seasim)
- Comprehensive Calibration and test reports
- Automation for PCIe PLL bandwidth and Peaking tests (including SJ calibration) for Gen 3.0/4.0/5.0/6.0

Tektronix is registered to ISO 9001:2015 and ISO 14001:2015.

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